

ZEKE Board User Manual

Revision 0.2

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Contents

Contents	1
List of Figures	3
Overview	5
Package Contents	5
Board Overview	6
Design Specification	7
Block Diagram	7
Power Supply	8
Power Management	8
FPGA	9
FPGA Power	9
FPGA Configuration	9
JTAG	10
Mode Setting	10
Clock Source	11
Reset System	12
EPCQ	13
Indirect Programming	13
Direct Programming	13
Linux Programming	13
DDR3	14
MicroSD Card	14
QSPI Flash	15
Ethernet	15
EtherCAT	16
LED, Switch, and Jumper	17
Expansion IO	19
Expansion Connection Table	19
FPGA Pin Summary	21
FPGA Connection Table	21
Start Using ZEKE	26
Power Up ZEKE Board	26
Step of Creating HPS on QSYS	26
Step of Generating SOF File	30
Step of Creating JIC File	32
Step of Programming by JTAG	34

Associated Product _____ **35**

 OSCAR Board _____ **35**

Additional Information _____ **36**

 Getting Help _____ **36**

 Revision History _____ **36**

List of Figures

Figure 1 : The ZEKE Board	5
Figure 2 : Top View of ZEKE Board	6
Figure 3 : Bottom View of ZEKE Board.....	6
Figure 4 : Block Diagram	7
Figure 5 : Power Block Diagram.....	8
Figure 6 : Power Sequence Diagram	8
Figure 7 : FPGA Configuration	9
Figure 8 : JTAG Connection	10
Figure 9 : Mode Setting Configuration	10
Figure 10 : Mode Setting Table.....	11
Figure 11 : Mode Controller.....	11
Figure 12 : Clock Source.....	11
Figure 13 : Reset System.....	12
Figure 14 : Example of Resetting by FPGA_CONF_DONE	12
Figure 15 : Indirect Programming	13
Figure 16 : Direct Programming.....	13
Figure 17 : DDR3	14
Figure 18 : MicroSD Card.....	14
Figure 19 : QSPI Flash	15
Figure 20 : Ethernet Connection	15
Figure 21 : Ethernet Address.....	15
Figure 22 : Ethernet Pin Description	16
Figure 23 : EtherCAT Connection	16
Figure 24 : EtherCAT Address.....	16
Figure 25 : EtherCAT Pin Description.....	16
Figure 26 : LED and Switch.....	17
Figure 27 : JTAG Chain Switch Control.....	17
Figure 28 : Jumper.....	18
Figure 29 : Power LED	18
Figure 30 : EtherCAT Speed LED	18
Figure 31 : Expansion Connector 1 (CN4).....	19
Figure 32 : Expansion Connector 2 (CN9).....	20
Figure 33 : FPGA Connection Summary	25

Figure 34 : Location of ZEKE Power	26
Figure 35 : QSYS Menu.....	27
Figure 36 : HPS on IP Catalog	27
Figure 37 : Arria V/Cyclone V Hard Processor System.....	28
Figure 38 : Peripheral Pins of HPS.....	28
Figure 39 : SDRAM of HPS.....	29
Figure 40 : HPS Design on QSYS.....	29
Figure 41 : QSYS Generate File.....	30
Figure 42 : Settings Menu in Quartus Prime	30
Figure 43 : Add File to Project	31
Figure 44 : Start Compilation	31
Figure 45 : SOF Output File.....	31
Figure 46 : Convet Programming Files Menu.....	32
Figure 47 : Programming File Type	32
Figure 48 : Setting SOF File and Flash Loader.....	33
Figure 49 : JIC Output File.....	33
Figure 50 : Programmer Menu	34
Figure 51 : Progeammer Device Setup.....	34
Figure 52 : Program the ZEKE board	35
Figure 53 : OSCAR Board	35

Overview



Figure 1 : The ZEKE Board

ZEKE board is an evaluation board which contains Cyclone V System-on-Chip (SoC), DDR3 memory, two of 10/100/1000 Ethernet (PHY), two of 10/100 Ethernet (PHY), MicroSD Card connector, NOR flash memory along with user IO such as DIP switch, LED, and expansion connector.

The Cyclone V SoC has ARM Cortex A9 Hard Processor System (HPS) and FPGA separately in a single chip. Two of 10/100/1000 Ethernet (PHY) and two of 10/100 Ethernet (PHY) enable implementation of various network communications such as Ethernet and EtherCAT. User IO and expansion connector allow user to use ZEKE board to control the other device or board depending on user application.

MicroSD Card connector and NOR flash memory directly connect to HPS core which allow user to freely store application software or up to operating system (OS) for CPU to work accordingly.

Package Contents

- ZEKE Board
- ZEKE Board User Manual
- 5V DC Power Supply

Board Overview

The components on the ZEKE board are shown in the Figure below.

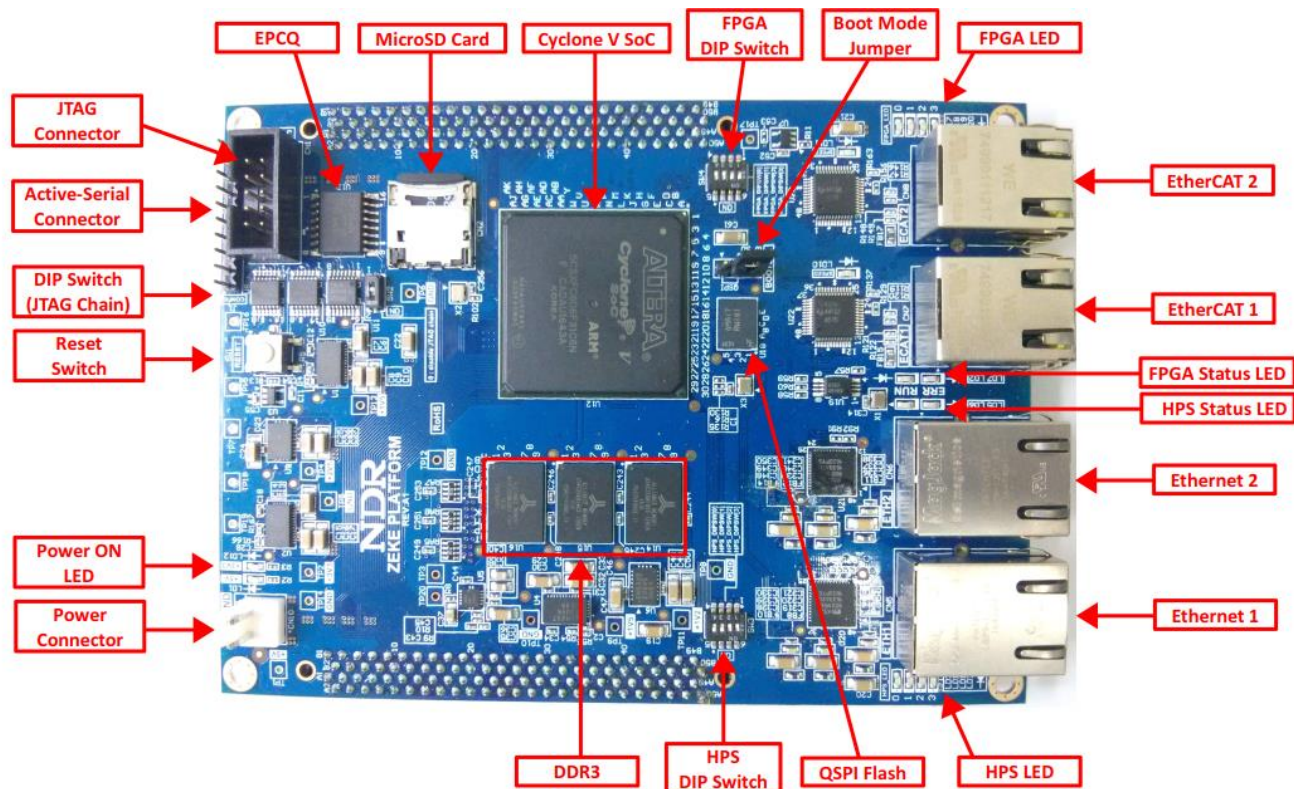


Figure 2 : Top View of ZEKE Board

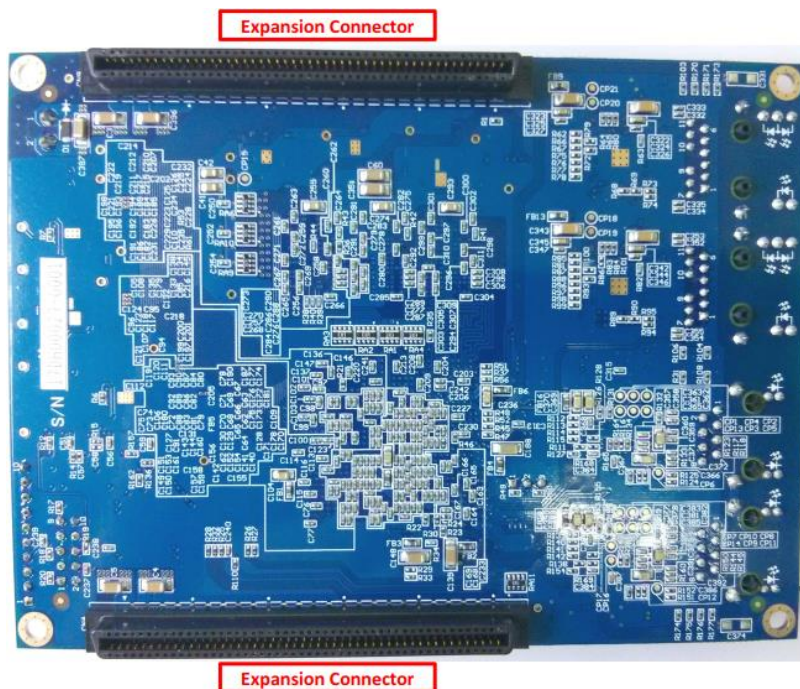


Figure 3 : Bottom View of ZEKE Board

Design Specification

- Power Connector : B2P-VH(LF)(SN)
- FPGA : 5CSXFC6D6F31C6N (Cyclone V SoC)
- EPCQ : EPCQ64SI16N (for FPGA)
- DDR3 x3 : 256Mb x 32
- SD Card : MicroSD Card
- QSPI Flash : MT25QL512ABB8E12-0SIT (QSPI for HPS)
- Ethernet x2 : KSZ9021RNI (Connect to HPS)
- EtherCAT x2 : TLK110PTR (Connect to FPGA)
- LED : IO LED x8, Status LED x6, Power LED x2
- DIP Switch : 4 channels x2, 1 channel x1
- Button Switch : Reset switch
- Jumper : 3 pins header for boot mode
- Expansion IO x2 : FX2C-100S-1.27DSA (FPGA IO + HPS IO + UART + Power)

Block Diagram

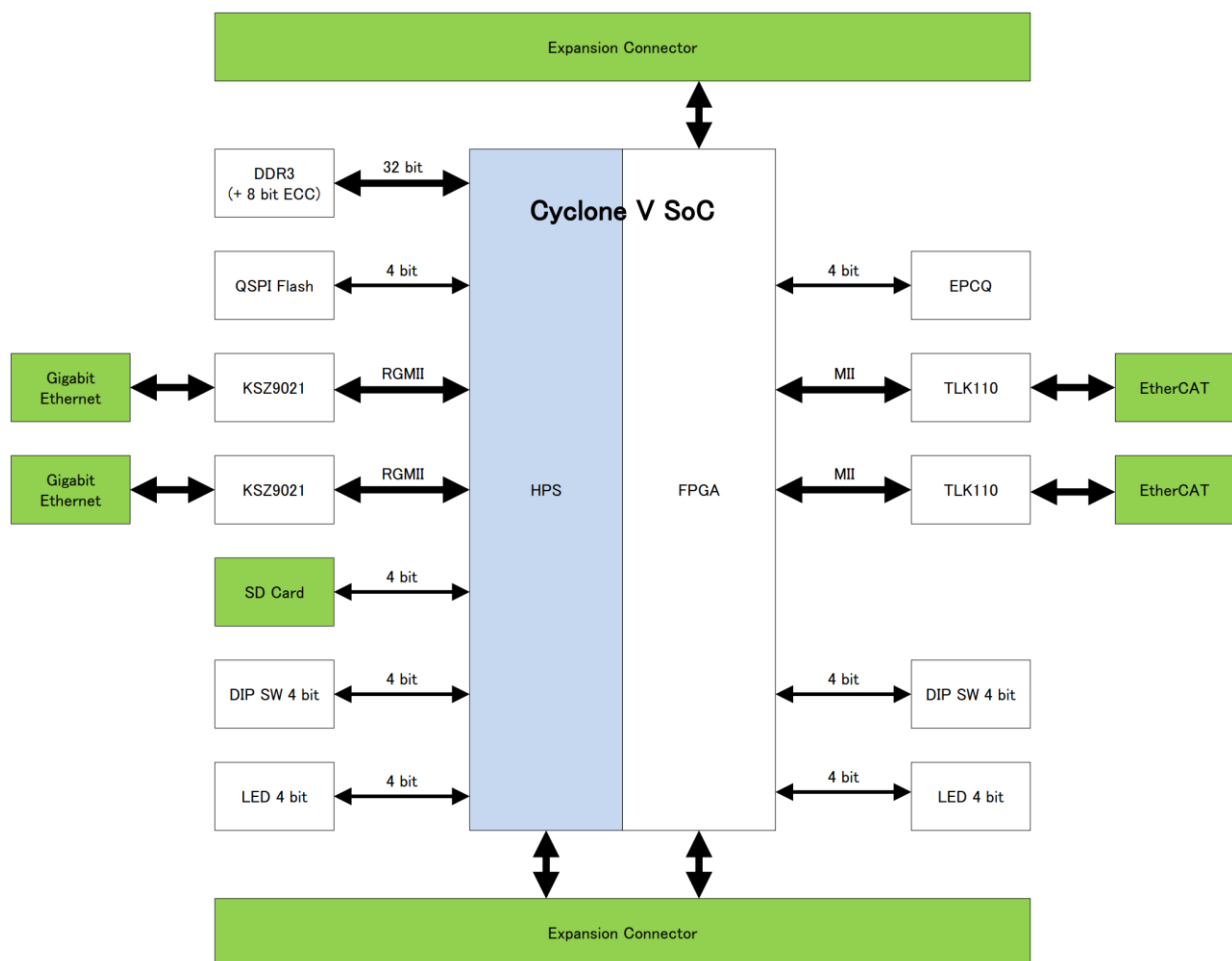


Figure 4 : Block Diagram

Power Supply

The ZEKE board is applied 5V power supply that recommend using at least 2A (output current of power supply). The connector of the power input is a 2-position header connector (CN10), and the part number is B2P-VH(LF)(SN). After plug the power supply in, the power LEDs (LD1 and LD12), that is beside of power connector, should be bright.

Power Management

The ZEKE board is applied 5V power supply, and generates voltage for the other components on the board. The DCDC converters and LDO regulator are used to regulate input voltage 5V to voltage level 0.75V, 1.1V, 1.2V, 1.5V, 2.5V, and 3.3V. There is the power sequence of the board. Firstly, 5V supplies to DCDC converter 1.1V, and then the DCDC converter generates 1.1V with Power OK (POK) signal. The POK is used to enable the other DCDC converters to generate the other voltage levels. The Figure 5 shows the power management structure and the power sequence. The Figure 6 shows the power sequence in timing diagram.

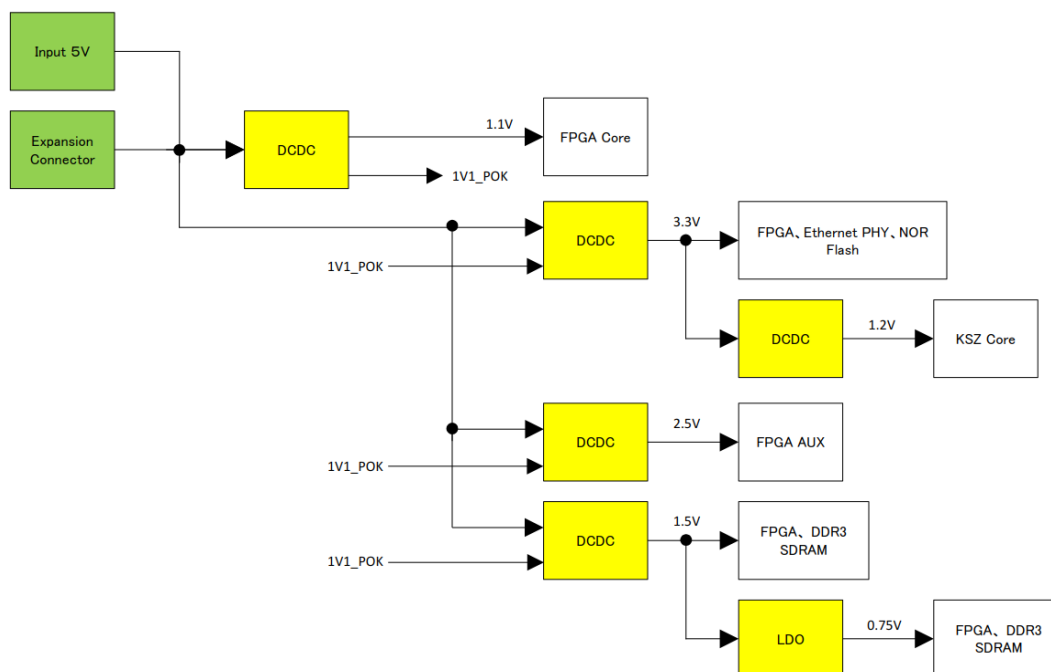


Figure 5 : Power Block Diagram

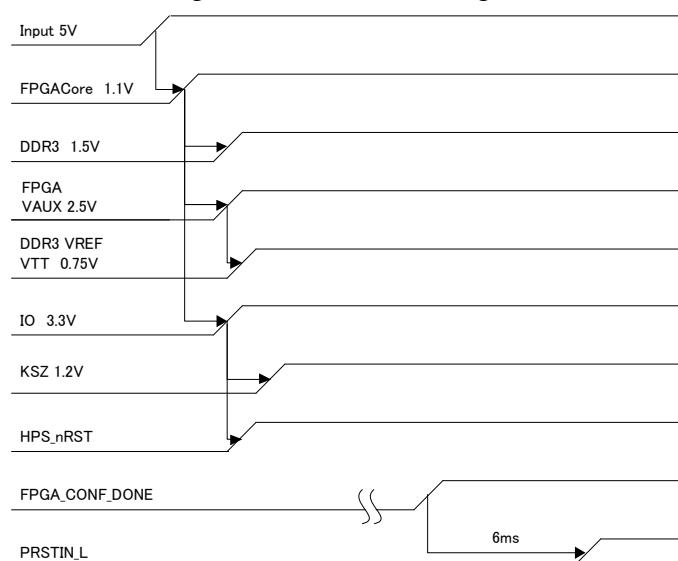


Figure 6 : Power Sequence Diagram

The ZEKE board uses Cyclone V SoC (5CSXFC6D6F31C6N) to be the main controller. This Cyclone V SoC has Hard Processor System (HPS) with ARM Cortex A9. For the summary of Cyclone V pin,

FPGA Power

The voltage level of Cyclone V SoC is designed in each bank following by the list below.

- Bank 3-5 and 7-8 : 3.3V
- Bank 6 : 1.5V (This bank is designed to control DDR and HPS DIP Switch)

FPGA Configuration

- nCONFIG = '1' : Normally no hard reset
- nCE = '0' : Normally always enable the chip
- MSEL[4..0] = "10010" : AS fast mode (Switch to standard mode by pull up MSEL[0])
- DEV_CLR = Not connected : Not using clear register function.
- DEV_OE = Not connected : Not using default IO state.
- BOOTSEL[2..0] = "1-1" : Boot from QSPI by pull up "111" and SD card by pull down "101" on J3
- CLKSEL[1..0] = "00" : Boot clock from osc1_clk / 4.

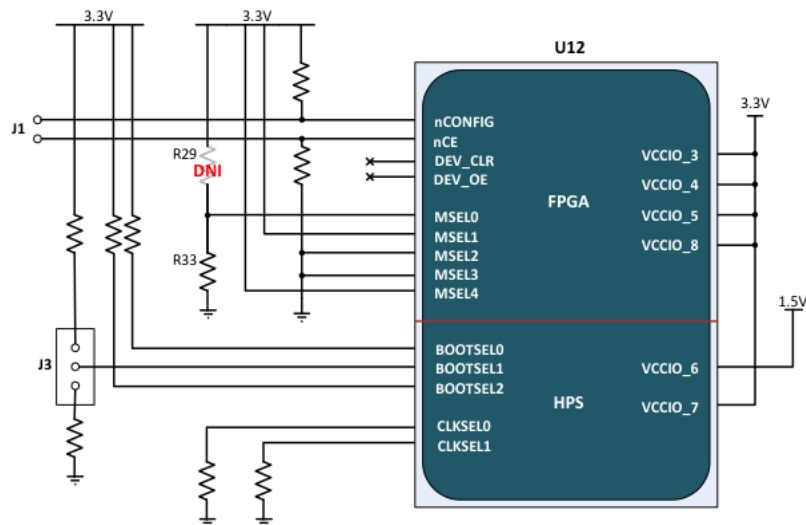


Figure 7 : FPGA Configuration

Note : Do Not Install (DNI) means that this part is not mounted for default.

JTAG

To program FPGA and HPS, you can program via JTAG connector (CN1) by enable JTAG chain on SW2 as shown in the Figure 8. To enable or disable JTAG chain, use SW2 by switching to OFF for enable and ON for disable.

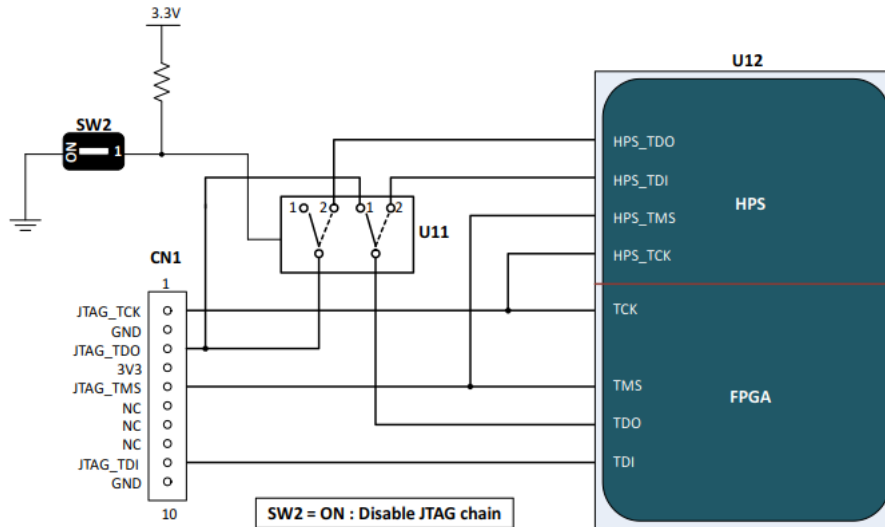


Figure 8 : JTAG Connection

Mode Setting

The mode setting on the ZEKE board has two type of setting mode, that are, configuration scheme (MSEL[4..0]) on FPGA and boot configuration on HPS as shown in the Figure 9.

For FPGA side, MSEL is fixed to AS configuration with fast Power-On Reset (POR) Delay, and the logic of MSEL is “10010”. MSEL can fix to the AS configuration with standard POR delay by switching the installation between resistor R29 and R33 of MSEL[0] so the logic will be “10011” for standard POR delay. Since the configuration scheme is selected to the AS configuration, JTAG-base configuration is also selected.

For HPS side, the boot configuration is divided to clock select field (CLKSEL[1..0]) and boot select field (BOOTSEL[2..0]). CLKSEL is clock selection for booting, and it is set to “00” that means the clock selection for booting is osc1_clk divided by 4. BOOTSEL is used to define the source of booting. BOOTSEL can be selected to “101” for booting from MicroSD Card and “111” for booting from QSPI flash. You can select BOOTSEL[1] by jumper (J3), and there are SD label and QSPI label beside J3.

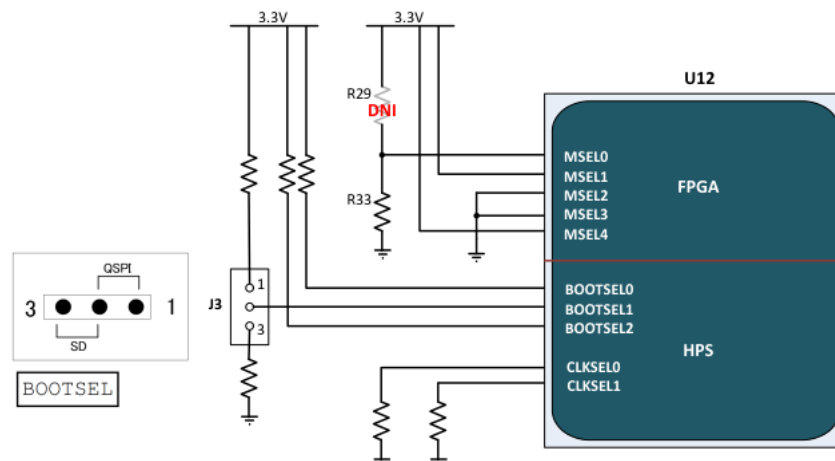


Figure 9 : Mode Setting Configuration

Signal	Descriptions	POR Delay	Mode Select
MSEL[4..0]	AS (x1 and x4)	Fast	"10010"
		Standard	"10011"
	JTAG-Base Configuration	–	Use MSEL setting above
BOOTSEL[2..0]	SD/MMC Internal Transceiver	–	"101"
	QSPI Flash	–	"111"
CLKSEL[1..0]	QSPI clock is $oscl_clk/4$, SD/MMC clock is $oscl_clk/4$, NAND clock is $oscl_clk/25$	–	"00"

Figure 10 : Mode Setting Table

Mode Setting	Logic Level	Controller
MSEL[4]	'1'	fixed
MSEL[3]	'0'	fixed
MSEL[2]	'0'	fixed
MSEL[1]	'1'	fixed
MSEL[0]	–	R29, R33
BOOTSEL[2]	'1'	fixed
BOOTSEL[1]	–	J3
BOOTSEL[0]	'1'	fixed
CLKSEL[1]	'0'	fixed
CLKSEL[0]	'0'	fixed

Figure 11 : Mode Controller

Clock Source

The ZEKE board has three clock sources for FPGA, HPS, and four Ethernet PHY chips. All clock sources are the same part number (SG-210STF25.000000MHzL), and the frequency is 25MHz with 50 ppm. The clock source of Ethernet PHY chip uses clock buffer to drive each Ethernet PHY chip. The block diagram in the Figure 12 shows the direction of these three clock sources.

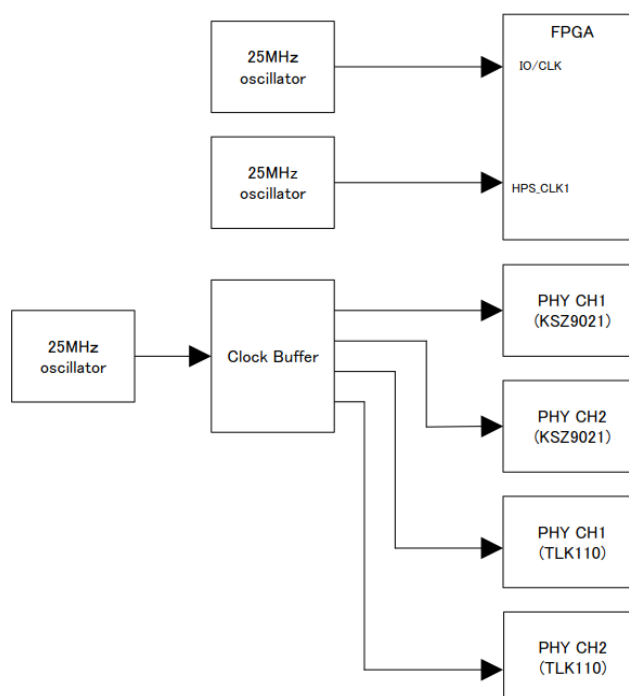


Figure 12 : Clock Source

Reset System

The ZEKE board has three choices to reset the system by following the list below. The reset time is about 6 ms that is made by reset IC (BU4245G-TR) with detection voltage 4.5V. The reset system is shown in the Figure 13.

1. ON/OFF power supply
2. Reset switch (SW1)
3. JTAG by resetting CONF_DONE pin

If you want to reset EtherCAT PHY (TLK110), you can reset by driving FPGA IO pin D7 (IO_T24n) to low logic level. Then, EtherCAT PHY will be reset.

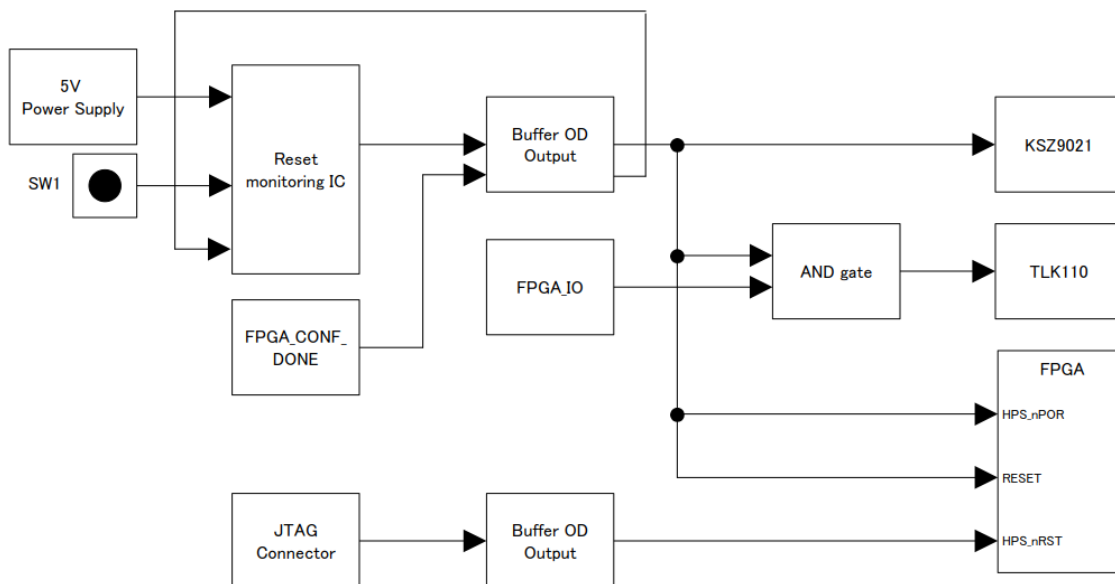


Figure 13 : Reset System

To reset by ON/OFF power supply, the reset IC detects the voltage level 4.5V, and then delay the time about 6 ms. SW1 and FPGA_CONF_DONE signal can also control the reset IC. The reset signal that is generated by the reset IC is PRSTIN_L. The example of timing is shown in the Figure 14.

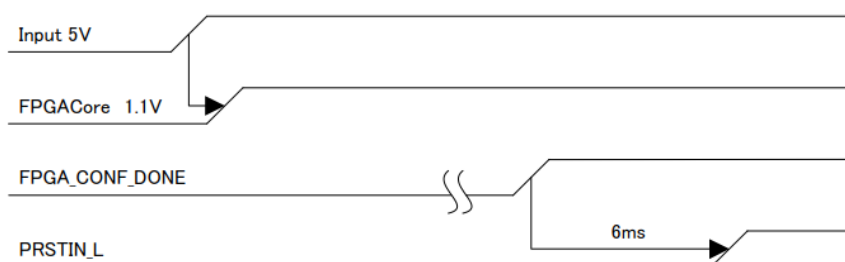


Figure 14 : Example of Resetting by FPGA_CONF_DONE

Quad-Serial Configuration (EPCQ) 64Mbit is a non-volatile memory, and used to save the configuration file on FPGA side. The part number is EPCQ64SI16N. The ZEKE board is designed to program EPCQ by three ways, that are, indirect programming, direct programming, and Linux programming.

Indirect Programming

The indirect programming uses JTAG interface. To program this way, you have to connect USB Blaster to JTAG connector (CN1) as shown in Figure 15, and enable the JTAG chain by swithing SW2 to OFF.

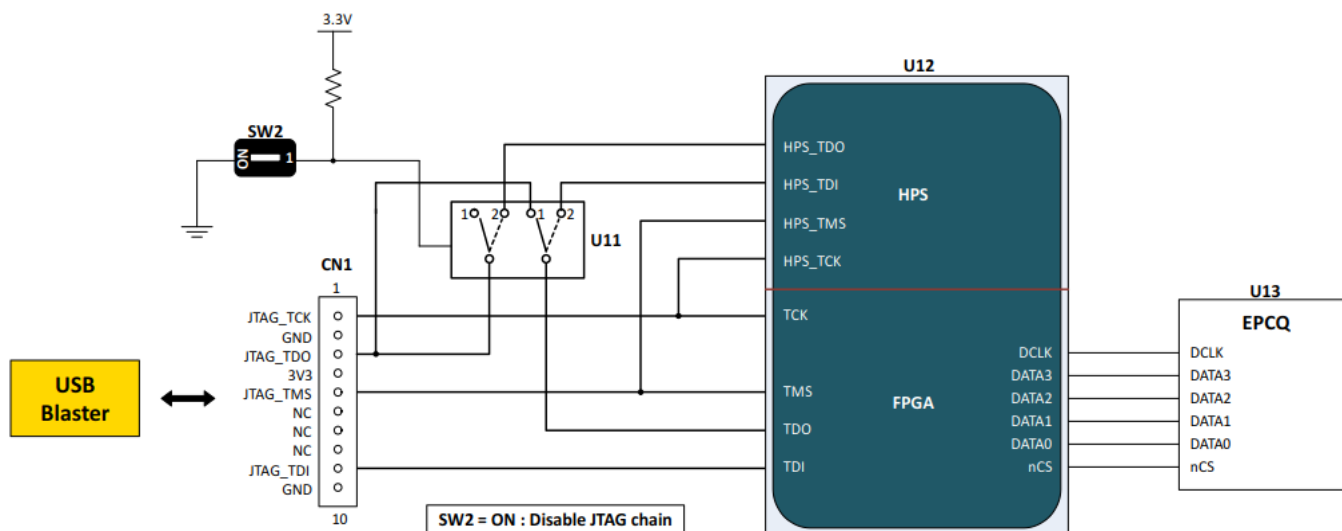


Figure 15 : Indirect Programming

Direct Programming

The direct programming uses the Active-Serial (AS) interface. Connect USB Blaster to header connector (J1) to program as shown in Figure 16.

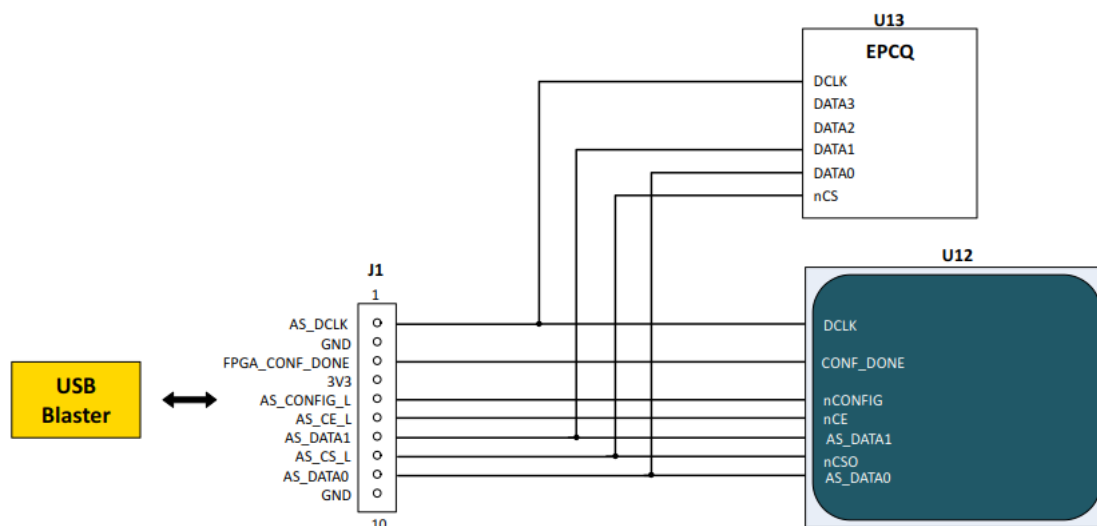


Figure 16 : Direct Programming

Linux Programming

The Linux programming is programming method that can program EPCQ by using MicroSD Card. Slot the MicroSD Card in to CN2, and then power up the ZEKE board. The EPCQ will be programmed by HPS.

DDR3

The ZEKE board includes three DDR3s 4Gb (256M x 16). The two of DDR3s are designed to be a simple RAM, and the another one is designed to be an Error-Correction Code memory (ECC memory). The total capacity of the memory is 8Gb (256M x 32). The DDR3s are connected to the hard memory controller in the HPS. The DDR3s use voltage level 1.5V SSTL-compatible inputs, and the speed grade of DDR3s interface is DDR3-1600.

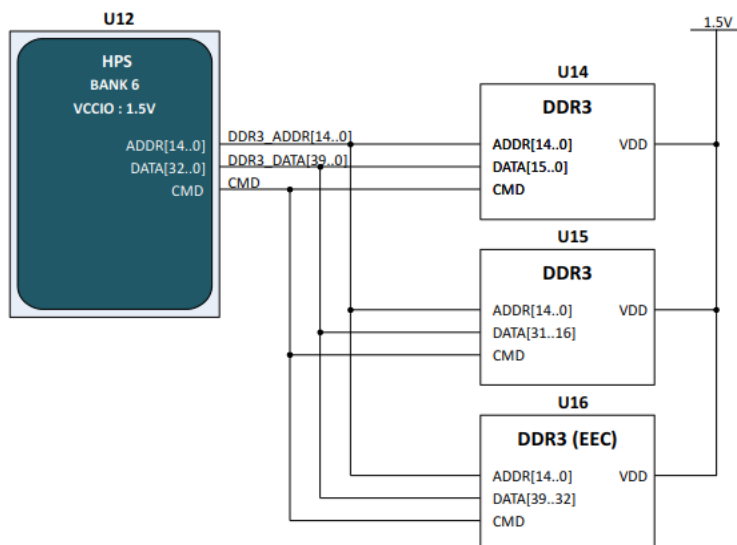


Figure 17 : DDR3

MicroSD Card

MicroSD Card slot (CN2) on the board is connected to HPS for booting Linux. The 4-bit data and the command of SD mode is used to access the MicroSD Card. To boot from MicroSD Card, slot the SD Card in, and set the mode selection for booting from MicroSD Card on J3 (pull-down on J3).

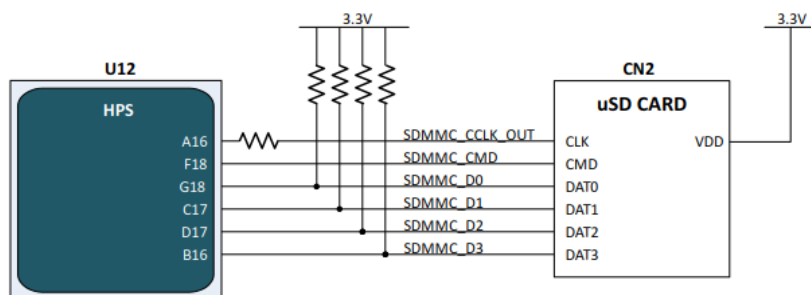


Figure 18 : MicroSD Card

QSPI Flash

On the HPS side, QSPI (MT25QL512ABB8E12-0SIT) 512Mbit is used to save the program file for booting HPS. The QSPI flash can be programmed by JTAG interface or MicroSD Card. To program the QSPI flash via JTAG interface, DON'T forget to switch the SW2 to OFF (enable JTAG chain) and select QSPI mode on J3 (pull-up on J3).

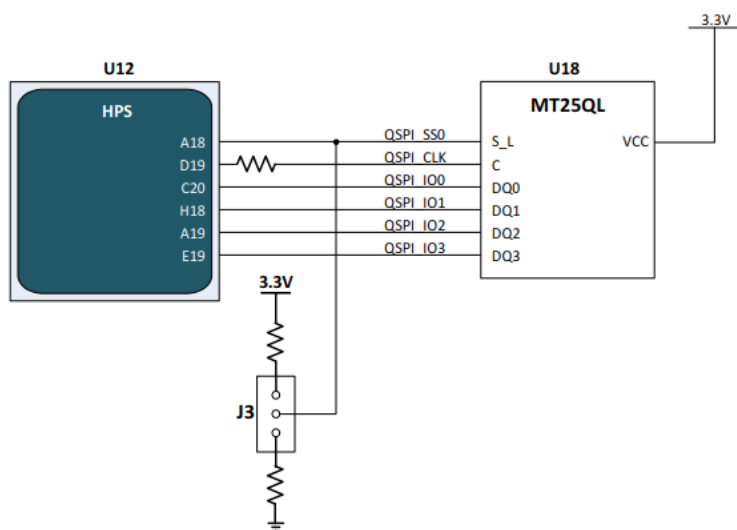


Figure 19 : QSPI Flash

Ethernet

Ehternet PHY chips (KSZ9021RNI) are used to design on the ZEKE board to be a Gigabit Ethernet transceiver with RGMII support. The ZEKE board has two Ethernet PHY chips that are connected to the hard Ethernet controller in the HPS (3.3V). After power-up, the Ethernet PHY starts with auto negotiation enabled, advertising 10/100/1000 link speeds and full duplex.

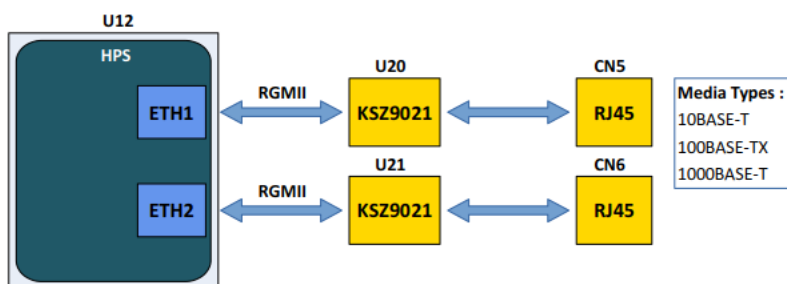


Figure 20 : Ethernet Connection

	Ethernet1	Ethernet2
PHYAD[4..0]	"00100"	"00110"

Figure 21 : Ethernet Address

Cyclone V Pin1	Ethernet1	Cyclone V Pin2	Ethernet2
B21	HPS_ETH_MDC	C14	HPS_ETH2_MDC
E21	HPS_ETH_MDIO	D15	HPS_ETH2_MDIO
C19	HPS_ETH_INT_L	B17	HPS_ETH2_INT_L
G20	HPS_ETH_RX_CLK	N16	HPS_ETH2_RX_CLK
K17	HPS_ETH_RX_CTL	M17	HPS_ETH2_RX_CTL
A21	HPS_ETH_RXD0	A15	HPS_ETH2_RXD0
B20	HPS_ETH_RXD1	C15	HPS_ETH2_RXD1
B18	HPS_ETH_RXD2	E14	HPS_ETH2_RXD2
D21	HPS_ETH_RXD3	A14	HPS_ETH2_RXD3
H19	HPS_ETH_TX_CLK	F16	HPS_ETH2_TX_CLK
A20	HPS_ETH_TX_CTL	B15	HPS_ETH2_TX_CTL
F20	HPS_ETH_TXD0	E16	HPS_ETH2_TXD0
J19	HPS_ETH_TXD1	G16	HPS_ETH2_TXD1
F21	HPS_ETH_TXD2	D16	HPS_ETH2_TXD2
F19	HPS_ETH_TXD3	D14	HPS_ETH2_TXD3

Figure 22 : Ethernet Pin Description

EtherCAT

EtherCAT PHY chips (TLK110PTR) are used to design on the ZEKE board to interface with EtherCAT. The EtherCAT PHY is 10/100Mbps Ethernet physical layer transceiver. There are two EtherCAT PHY chips on the ZEKE board, and both are connected to the FPGA (3.3V) bank 8. After power-up, the EtherCAT PHY starts with auto negotiation enabled, advertising 10/100 link speeds and full duplex. The list of pin connection is shown below.

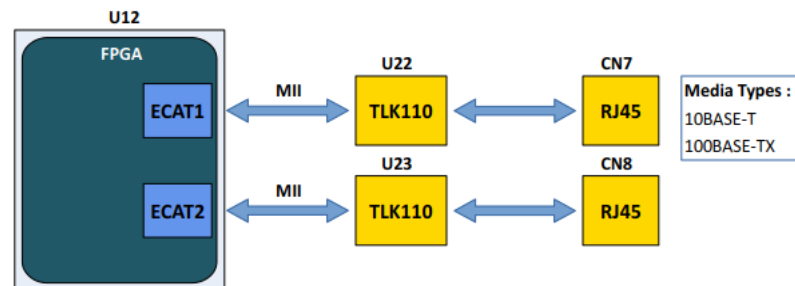


Figure 23 : EtherCAT Connection

	EtherCAT1	EtherCAT2
PHYAD[4..0]	"00001"	"00011"

Figure 24 : EtherCAT Address

Cyclone V Pin1	EtherCAT1	Cyclone V Pin2	EtherCAT2
D7	PHY1_2_RESET_L	D7	PHY1_2_RESET_L
D4	PHY1_2_MDCLK	D4	PHY1_2_MDCLK
D2	PHY1_2_MDIO	D2	PHY1_2_MDIO
D12	PHY1_COL	D5	PHY2_COL
C7	PHY1_CSR	D6	PHY2_CSR
D11	PHY1_INT_L	D1	PHY2_INT_L
C9	PHY1_RX_CLK	C4	PHY2_RX_CLK
C8	PHY1_RX_DV	C3	PHY2_RX_DV
C10	PHY1_RX_ER	C2	PHY2_RX_ER
B8	PHY1_RXD[0]	B3	PHY2_RXD[0]
B7	PHY1_RXD[1]	B2	PHY2_RXD[1]
C13	PHY1_RXD[2]	B1	PHY2_RXD[2]
C12	PHY1_RXD[3]	C5	PHY2_RXD[3]
B12	PHY1_TX_CLK	B5	PHY2_TX_CLK
A13	PHY1_TXD[0]	A6	PHY2_TXD[0]
A9	PHY1_TXD[1]	A5	PHY2_TXD[1]
A8	PHY1_TXD[2]	A3	PHY2_TXD[2]
B13	PHY1_TXD[3]	A4	PHY2_TXD[3]
B11	PHY1_TXEN	B6	PHY2_TXEN
D10	PHY1_LINK	D9	PHY2_LINK

Figure 25 : EtherCAT Pin Description

LED, Switch, and Jumper

The Cyclone V includes 1 DIP switch 1 button switch and 6 LEDs on the FPGA, and 1 DIP switch and 6 LEDs on the HPS as shown in the Figure 26. The voltage level of FPGA switch is 3.3V, and the voltage level of HPS switch is 1.5V. The button switch is used to reset the system. The voltage level of all LEDs is 3.3V. The Cyclone V has to drive high logic to turn on the LEDs, and low logic to turn off the LEDs. For the DIP switches, the Cyclone V will detect low logic if switch the DIP switch to ON. The purpose of LED RUN and ERR is to show the status of EtherCAT and Ethernet.

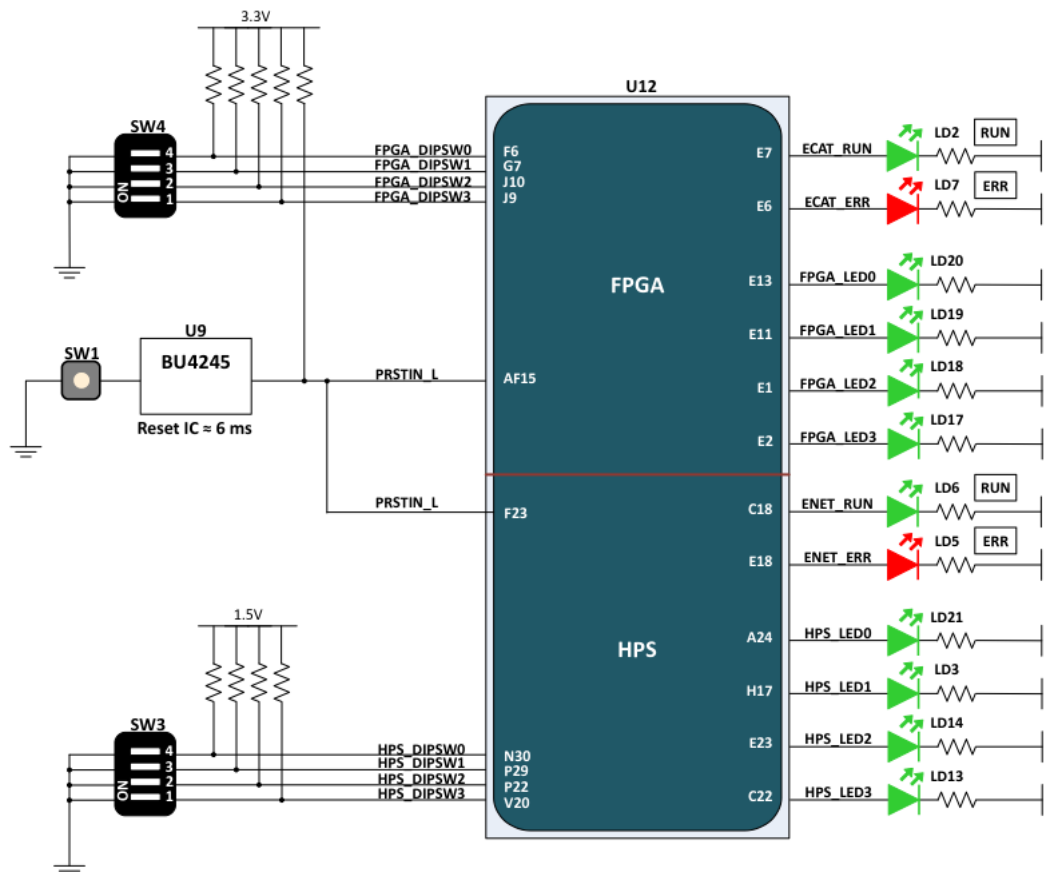


Figure 26 : LED and Switch

The 1 bit DIP switch (SW2) is used to enable and disable the JTAG chain as shown in the Figure 27. Switching to OFF is enable, and switching to ON is disable.

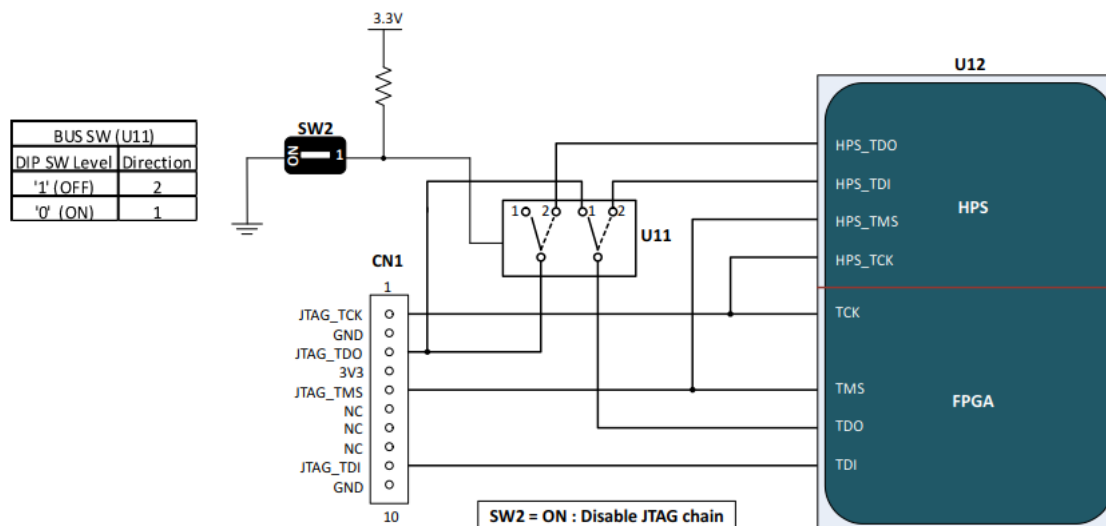


Figure 27 : JTAG Chain Switch Control

The Jumper (J3) on the ZEKE board is used to select the boot mode. Two boot sources are MicroSD Card and QSPI flash as shown in the Figure 28.

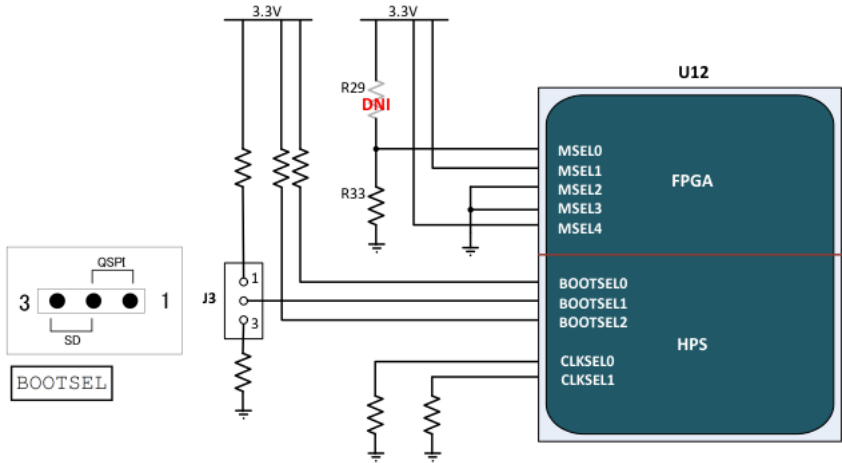


Figure 28 : Jumper

The two LEDs (LD1 and LD12) indicate the power of the ZEKE board to show that there is power supply 5V and 3.3V on the board or not as shown in the Figure 29.

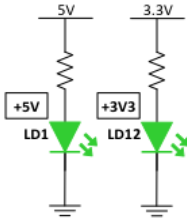


Figure 29 : Power LED

The other two LEDs (LD10 and LD11) show the speed of EtherCAT communication as shown in the Figure 30. If LED is ON, the link speed is 100Mbps. If LED is OFF, the speed is 10Mbps.

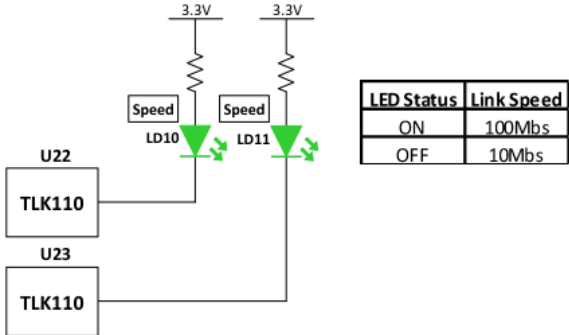


Figure 30 : EtherCAT Speed LED

Expansion IO

The ZEKE board has two expansion connectors on the bottom of the board. The IO pins are directly connected between the Cyclone V and the expansion connectors. Voltage level of all pins connection is 3.3V.

Expansion Connection Table

ZEKE CN4					
Cyclone V Pin	Signal name	CN4		Signal name	Cyclone V Pin
	5V	A1	B1	5V	
	5V	A2	B2	5V	
	3.3V	A3	B3	3.3V	
	3.3V	A4	B4	3.3V	
AE14	FPGA_GPIO[0]	A5	B5	FPGA_GPIO[1]	AE13
AH13	FPGA_GPIO[2]	A6	B6	FPGA_GPIO[3]	AG13
AF13	FPGA_GPIO[4]	A7	B7	FPGA_GPIO[5]	AH12
AG12	FPGA_GPIO[6]	A8	B8	FPGA_GPIO[7]	AE12
AG11	FPGA_GPIO[8]	A9	B9	FPGA_GPIO[9]	AF11
	GND	A10	B10	GND	
AH10	FPGA_GPIO[10]	A11	B11	FPGA_GPIO[11]	AG10
AF10	FPGA_GPIO[12]	A12	B12	FPGA_GPIO[13]	AH9
AF9	FPGA_GPIO[14]	A13	B13	FPGA_GPIO[15]	AH8
AH7	FPGA_GPIO[16]	A14	B14	FPGA_GPIO[17]	AG8
AG7	FPGA_GPIO[18]	A15	B15	FPGA_GPIO[19]	AF8
AG6	FPGA_GPIO[20]	A16	B16	FPGA_GPIO[21]	AH5
AH4	FPGA_GPIO[22]	A17	B17	FPGA_GPIO[23]	AH3
AG5	FPGA_GPIO[24]	A18	B18	FPGA_GPIO[25]	AG3
AF6	FPGA_GPIO[26]	A19	B19	FPGA_GPIO[27]	AF5
	GND	A20	B20	GND	
AJ10	FPGA_GPIO[28]	A21	B21	FPGA_GPIO[29]	AK9
AJ9	FPGA_GPIO[30]	A22	B22	FPGA_GPIO[31]	AK8
AK7	FPGA_GPIO[32]	A23	B23	FPGA_GPIO[33]	AJ7
AK6	FPGA_GPIO[34]	A24	B24	FPGA_GPIO[35]	AJ6
AJ5	FPGA_GPIO[36]	A25	B25	FPGA_GPIO[37]	AK4
AJ4	FPGA_GPIO[38]	A26	B26	FPGA_GPIO[39]	AK3
AK2	FPGA_GPIO[40]	A27	B27	FPGA_GPIO[41]	AJ2
AJ1	FPGA_GPIO[42]	A28	B28	FPGA_GPIO[43]	AH2
AG2	FPGA_GPIO[44]	A29	B29	FPGA_GPIO[45]	AG1
	GND	A30	B30	GND	
AF4	FPGA_GPIO[46]	A31	B31	FPGA_GPIO[47]	AE9
AE7	FPGA_GPIO[48]	A32	B32	FPGA_GPIO[49]	AD7
AD9	FPGA_GPIO[50]	A33	B33	FPGA_GPIO[51]	AE11
AC9	FPGA_GPIO[52]	A34	B34	FPGA_GPIO[53]	AD11
AD12	FPGA_GPIO[54]	A35	B35	FPGA_GPIO[55]	AD14
AC12	FPGA_GPIO[56]	A36	B36	FPGA_GPIO[57]	AC14
AB15	FPGA_GPIO[58]	A37	B37	FPGA_GPIO[59]	AB12
AA12	FPGA_GPIO[60]	A38	B38	FPGA_GPIO[61]	AB13
AA13	FPGA_GPIO[62]	A39	B39	FPGA_GPIO[63]	AA14
	GND	A40	B40	GND	
AA15	FPGA_GPIO[64]	A41	B41	FPGA_GPIO[65]	W15
K14	FPGA_GPIO[66]	A42	B42	FPGA_GPIO[67]	J14
H15	FPGA_GPIO[68]	A43	B43	FPGA_GPIO[69]	G15
F15	FPGA_GPIO[70]	A44	B44	FPGA_GPIO[71]	F14
K8	FPGA_GPIO[72]	A45	B45	FPGA_GPIO[73]	F13
G12	FPGA_GPIO[74]	A46	B46	FPGA_GPIO[75]	G11
G10	FPGA_GPIO[76]	A47	B47	FPGA_GPIO[77]	G8
F11	FPGA_GPIO[78]	A48	B48	FPGA_GPIO[79]	F10
E9	FPGA_GPIO[80]	A49	B49	FPGA_GPIO[81]	E8
E3	FPGA_GPIO[82]	A50	B50	FPGA_GPIO[83]	E4

Figure 31 : Expansion Connector 1 (CN4)

ZEKE CN9					
Cyclone V Pin	Signal name	CN9		Signal name	Cyclone V Pin
	5V	A1	B1	5V	
	5V	A2	B2	5V	
	3.3V	A3	B3	3.3V	
	3.3V	A4	B4	3.3V	
AG22	FPGA_GPIO[84]	A5	B5	FPGA_GPIO[85]	AH22
AG23	FPGA_GPIO[86]	A6	B6	FPGA_GPIO[87]	AH23
AE19	FPGA_GPIO[88]	A7	B7	FPGA_GPIO[89]	AD17
AH24	FPGA_GPIO[90]	A8	B8	FPGA_GPIO[91]	AF24
AJ11	FPGA_GPIO[92]	A9	B9	FPGA_GPIO[93]	AK11
	GND	A10	B10	GND	
AJ12	FPGA_GPIO[94]	A11	B11	FPGA_GPIO[95]	AK12
AK13	FPGA_GPIO[96]	A12	B12	FPGA_GPIO[97]	AJ14
AK14	FPGA_GPIO[98]	A13	B13	FPGA_GPIO[99]	AK16
AJ16	FPGA_GPIO[100]	A14	B14	FPGA_GPIO[101]	AJ17
AK23	FPGA_GPIO[102]	A15	B15	FPGA_GPIO[103]	AK24
AJ24	FPGA_GPIO[104]	A16	B16	FPGA_GPIO[105]	AJ25
AF16	FPGA_GPIO[106]	A17	B17	FPGA_GPIO[107]	AG16
AH17	FPGA_GPIO[108]	A18	B18	FPGA_GPIO[109]	AE17
AG18	FPGA_GPIO[110]	A19	B19	FPGA_GPIO[111]	AH18
	GND	A20	B20	GND	
AF18	FPGA_GPIO[112]	A21	B21	FPGA_GPIO[113]	AF19
AK26	FPGA_GPIO[114]	A22	B22	FPGA_GPIO[115]	AJ26
AJ27	FPGA_GPIO[116]	A23	B23	FPGA_GPIO[117]	AK27
AH27	FPGA_GPIO[118]	A24	B24	FPGA_GPIO[119]	AH28
AK28	FPGA_GPIO[120]	A25	B25	FPGA_GPIO[121]	AK29
AH29	FPGA_GPIO[122]	A26	B26	FPGA_GPIO[123]	AH30
AG30	FPGA_GPIO[124]	A27	B27	FPGA_GPIO[125]	AF30
AH19	FPGA_GPIO[126]	A28	B28	FPGA_GPIO[127]	AH20
AF20	FPGA_GPIO[128]	A29	B29	FPGA_GPIO[129]	AG20
	GND	A30	B30	GND	
AK18	FPGA_GPIO[130]	A31	B31	FPGA_GPIO[131]	AK19
AJ19	FPGA_GPIO[132]	A32	B32	FPGA_GPIO[133]	AJ20
AK21	FPGA_GPIO[134]	A33	B33	FPGA_GPIO[135]	AJ21
AK22	FPGA_GPIO[136]	A34	B34	FPGA_GPIO[137]	AJ22
AG21	FPGA_GPIO[138]	A35	B35	FPGA_GPIO[139]	AE18
AF21	FPGA_GPIO[140]	A36	B36	FPGA_GPIO[141]	AE23
AC18	FPGA_GPIO[142]	A37	B37	FPGA_GPIO[143]	AA16
AC20	FPGA_GPIO[144]	A38	B38	FPGA_GPIO[145]	AG26
AF26	FPGA_GPIO[146]	A39	B39	FPGA_GPIO[147]	AB17
	GND	A40	B40	GND	
Y16	FPGA_GPIO[148]	A41	B41	FPGA_GPIO[149]	AA19
W16	FPGA_GPIO[150]	A42	B42	FPGA_GPIO[151]	Y17
AA18	FPGA_GPIO[152]	A43	B43	FPGA_GPIO[153]	W17
Y18	FPGA_GPIO[154]	A44	B44	FPGA_GPIO[155]	W19
V16	FPGA_GPIO[156]	A45	B45	FPGA_GPIO[157]	V17
B26 (GPIO48)	HPS_GPIO[0]	A46	B46	HPS_GPIO[1]	B25 (GPIO49)
A25 (GPIO51)	HPS_GPIO[2]	A47	B47	HPS_GPIO[3]	C25 (GPIO50)
H20 (SPIM0_SS0)	HPS_GPIO[4]	A48	B48	HPS_GPIO[5]	B23 (GPIO59)
G22 (GPIO62)	HPS_GPIO[6]	A49	B49	HPS_GPIO[7]	B22 (GPIO61)
C23 (GPIO63)	HPS_UART_RX	A50	B50	HPS_UART_TX	D22 (GPIO64)

Figure 32 : Expansion Connector 2 (CN9)

FPGA Pin Summary

This is the summary of FPGA pin. For more detail please see on Schematic of ZEKE board.

FPGA Connection Table

Signal name	Cyclone V Pin	Signal name	Cyclone V Pin
FPGA_CLK	AF14	DDR3	
HPS_CLK1	D25	DDR3_DATA[0]	K23
HPS_CLK2	F25	DDR3_DATA[1]	K22
PRSTIN_L	AF15	DDR3_DATA[2]	H30
HPS_RST_L	C27	DDR3_DATA[3]	G28
CV_JTAG_TCK	AC5	DDR3_DATA[4]	L25
CV_JTAG_TDI	U8	DDR3_DATA[5]	L24
CV_JTAG_TDO	AB9	DDR3_DATA[6]	J30
CV_JTAG_TMS	A29	DDR3_DATA[7]	J29
FPGA_JTAG_TDO	B27	DDR3_DATA[8]	K26
HPS_JTAG_TDO	B28	DDR3_DATA[9]	L26
FPGA_CONF_DONE	F3	DDR3_DATA[10]	K29
AS_CE_L	G5	DDR3_DATA[11]	K27
AS_CONFIG_L	J5	DDR3_DATA[12]	M26
AS_CS_L	AB8	DDR3_DATA[13]	M27
AS_DATA0	AE6	DDR3_DATA[14]	L28
AS_DATA1	AE5	DDR3_DATA[15]	M30
AS_DATA2	AE8	DDR3_DATA[16]	U26
AS_DATA3	AC7	DDR3_DATA[17]	T26
AS_DCLK	U7	DDR3_DATA[18]	N29
DDR3		DDR3_DATA[19]	N28
DDR3_ADDR[0]	F26	DDR3_DATA[20]	P26
DDR3_ADDR[1]	G30	DDR3_DATA[21]	P27
DDR3_ADDR[2]	F28	DDR3_DATA[22]	N27
DDR3_ADDR[3]	F30	DDR3_DATA[23]	R29
DDR3_ADDR[4]	J25	DDR3_DATA[24]	P24
DDR3_ADDR[5]	J27	DDR3_DATA[25]	P25
DDR3_ADDR[6]	F29	DDR3_DATA[26]	T29
DDR3_ADDR[7]	E28	DDR3_DATA[27]	T28
DDR3_ADDR[8]	H27	DDR3_DATA[28]	R27
DDR3_ADDR[9]	G26	DDR3_DATA[29]	R26
DDR3_ADDR[10]	D29	DDR3_DATA[30]	V30
DDR3_ADDR[11]	C30	DDR3_DATA[31]	W29
DDR3_ADDR[12]	B30	DDR3_DATA[32]	W26
DDR3_ADDR[13]	C29	DDR3_DATA[33]	R24
DDR3_ADDR[14]	H25	DDR3_DATA[34]	U27
DDR3_BA0	E29	DDR3_DATA[35]	V28
DDR3_BA1	J24	DDR3_DATA[36]	T25
DDR3_BA2	J23	DDR3_DATA[37]	U25
DDR3_CAS_L	E27	DDR3_DATA[38]	V27
DDR3_CKE	L29	DDR3_DATA[39]	Y29
DDR3_CLK_N	L23	DDR3_DM0	K28
DDR3_CLK_P	M23	DDR3_DM1	M28
DDR3_CS_L	H24	DDR3_DM2	R28

Signal name	Cyclone V Pin	Signal name	Cyclone V Pin
DDR3		Ethernet	
DDR3_DM3	W30	HPS_ETH_TX_CTL	A20
DDR3_DM4	W27	HPS_ETH_TXD0	F20
DDR3_DQS0_N	M19	HPS_ETH_TXD1	J19
DDR3_DQS0_P	N18	HPS_ETH_TXD2	F21
DDR3_DQS1_N	N24	HPS_ETH_TXD3	F19
DDR3_DQS1_P	N25	HPS_ETH2_INT_L	B17
DDR3_DQS2_N	R18	HPS_ETH2_MDC	C14
DDR3_DQS2_P	R19	HPS_ETH2_MDIO	D15
DDR3_DQS3_N	R21	HPS_ETH2_RX_CLK	N16
DDR3_DQS3_P	R22	HPS_ETH2_RX_CTL	M17
DDR3_DQS4_N	T23	HPS_ETH2_RXD0	A15
DDR3_DQS4_P	T24	HPS_ETH2_RXD1	C15
DDR3_ODT	H28	HPS_ETH2_RXD2	E14
DDR3_RAS_L	D30	HPS_ETH2_RXD3	A14
DDR3_RESET_L	P30	HPS_ETH2_TX_CTL	B15
DDR3_WE_L	C28	HPS_ETH2_TXD0	E16
MicroSD Card		HPS_ETH2_TXD1	G16
HPS_SDIO_CMD	F18	HPS_ETH2_TXD2	D16
HPS_SDIO_D0	G18	HPS_ETH2_TXD3	D14
HPS_SDIO_D1	C17	EtherCAT	
HPS_SDIO_D2	D17	FPGA_PHY1_2_RESET_L	D7
HPS_SDIO_D3	B16	PHY1_2_MDCLK	D4
HPS_SDIO_CMD	F18	PHY1_2_MDIO	D2
HPS_SDIO_D0	G18	PHY1_COL	D12
HPS_SDIO_D1	C17	PHY1_CSR	C7
HPS_SDIO_D2	D17	PHY1_INT_L	D11
HPS_SDIO_D3	B16	PHY1_LINK	D10
QSPI Flash		PHY1_RX_CLK	C9
HPS_QSPI_IO0	C20	PHY1_RX_DV	C8
HPS_QSPI_IO1	H18	PHY1_RX_ER	C10
HPS_QSPI_IO2	A19	PHY1_RXD[0]	B8
HPS_QSPI_IO3	E19	PHY1_RXD[1]	B7
SS0_BOOTSEL1	A18	PHY1_RXD[2]	C13
Ethernet		PHY1_RXD[3]	C12
HPS_ETH_INT_L	C19	PHY1_TX_CLK	B12
HPS_ETH_MDC	B21	PHY1_TXD[0]	A13
HPS_ETH_MDIO	E21	PHY1_TXD[1]	A9
HPS_ETH_RX_CLK	G20	PHY1_TXD[2]	A8
HPS_ETH_RX_CTL	K17	PHY1_TXD[3]	B13
HPS_ETH_RXD0	A21	PHY1_TXEN	B11
HPS_ETH_RXD1	B20	PHY2_COL	D5
HPS_ETH_RXD2	B18	PHY2_CSR	D6
HPS_ETH_RXD3	D21	PHY2_INT_L	D1

Signal name	Cyclone V Pin	Signal name	Cyclone V Pin
EtherCAT		GPIO	
PHY2_LINK	D9	FPGA_GPIO[6]	AG12
PHY2_RX_CLK	C4	FPGA_GPIO[7]	AE12
PHY2_RX_DV	C3	FPGA_GPIO[8]	AG11
PHY2_RX_ER	C2	FPGA_GPIO[9]	AF11
PHY2_RXD[0]	B3	FPGA_GPIO[10]	AH10
PHY2_RXD[1]	B2	FPGA_GPIO[11]	AG10
PHY2_RXD[2]	B1	FPGA_GPIO[12]	AF10
PHY2_RXD[3]	C5	FPGA_GPIO[13]	AH9
PHY2_TX_CLK	B5	FPGA_GPIO[14]	AF9
PHY2_TXD[0]	A6	FPGA_GPIO[15]	AH8
PHY2_TXD[1]	A5	FPGA_GPIO[16]	AH7
PHY2_TXD[2]	A3	FPGA_GPIO[17]	AG8
PHY2_TXD[3]	A4	FPGA_GPIO[18]	AG7
PHY2_TXEN	B6	FPGA_GPIO[19]	AF8
LED		FPGA_GPIO[20]	AG6
ECAT_ERR	E6	FPGA_GPIO[21]	AH5
ECAT_RUN	E7	FPGA_GPIO[22]	AH4
ENET_ERR	E18	FPGA_GPIO[23]	AH3
ENET_RUN	C18	FPGA_GPIO[24]	AG5
FPGA_LED[0]	E13	FPGA_GPIO[25]	AG3
FPGA_LED[1]	E11	FPGA_GPIO[26]	AF6
FPGA_LED[2]	E1	FPGA_GPIO[27]	AF5
FPGA_LED[3]	E2	FPGA_GPIO[28]	AJ10
HPS_LED[0]	A24	FPGA_GPIO[29]	AK9
HPS_LED[1]	H17	FPGA_GPIO[30]	AJ9
HPS_LED[2]	E23	FPGA_GPIO[31]	AK8
HPS_LED[3]	C22	FPGA_GPIO[32]	AK7
DIP Switch		FPGA_GPIO[33]	AJ7
FPGA_DIPSW0	F6	FPGA_GPIO[34]	AK6
FPGA_DIPSW1	G7	FPGA_GPIO[35]	AJ6
FPGA_DIPSW2	J10	FPGA_GPIO[36]	AJ5
FPGA_DIPSW3	J9	FPGA_GPIO[37]	AK4
HPS_DIPSW0	N30	FPGA_GPIO[38]	AJ4
HPS_DIPSW1	P29	FPGA_GPIO[39]	AK3
HPS_DIPSW2	P22	FPGA_GPIO[40]	AK2
HPS_DIPSW3	V20	FPGA_GPIO[41]	AJ2
GPIO		FPGA_GPIO[42]	AJ1
FPGA_GPIO[0]	AE14	FPGA_GPIO[43]	AH2
FPGA_GPIO[1]	AE13	FPGA_GPIO[44]	AG2
FPGA_GPIO[2]	AH13	FPGA_GPIO[45]	AG1
FPGA_GPIO[3]	AG13	FPGA_GPIO[46]	AF4
FPGA_GPIO[4]	AF13	FPGA_GPIO[47]	AE9
FPGA_GPIO[5]	AH12	FPGA_GPIO[48]	AE7

Signal name	Cyclone V Pin	Signal name	Cyclone V Pin
GPIO		GPIO	
FPGA_GPIO[49]	AD7	FPGA_GPIO[92]	AJ11
FPGA_GPIO[50]	AD9	FPGA_GPIO[93]	AK11
FPGA_GPIO[51]	AE11	FPGA_GPIO[94]	AJ12
FPGA_GPIO[52]	AC9	FPGA_GPIO[95]	AK12
FPGA_GPIO[53]	AD11	FPGA_GPIO[96]	AK13
FPGA_GPIO[54]	AD12	FPGA_GPIO[97]	AJ14
FPGA_GPIO[55]	AD14	FPGA_GPIO[98]	AK14
FPGA_GPIO[56]	AC12	FPGA_GPIO[99]	AK16
FPGA_GPIO[57]	AC14	FPGA_GPIO[100]	AJ16
FPGA_GPIO[58]	AB15	FPGA_GPIO[101]	AJ17
FPGA_GPIO[59]	AB12	FPGA_GPIO[102]	AK23
FPGA_GPIO[60]	AA12	FPGA_GPIO[103]	AK24
FPGA_GPIO[61]	AB13	FPGA_GPIO[104]	AJ24
FPGA_GPIO[62]	AA13	FPGA_GPIO[105]	AJ25
FPGA_GPIO[63]	AA14	FPGA_GPIO[106]	AF16
FPGA_GPIO[64]	AA15	FPGA_GPIO[107]	AG16
FPGA_GPIO[65]	W15	FPGA_GPIO[108]	AH17
FPGA_GPIO[66]	K14	FPGA_GPIO[109]	AE17
FPGA_GPIO[67]	J14	FPGA_GPIO[110]	AG18
FPGA_GPIO[68]	H15	FPGA_GPIO[111]	AH18
FPGA_GPIO[69]	G15	FPGA_GPIO[112]	AF18
FPGA_GPIO[70]	F15	FPGA_GPIO[113]	AF19
FPGA_GPIO[71]	F14	FPGA_GPIO[114]	AK26
FPGA_GPIO[72]	K8	FPGA_GPIO[115]	AJ26
FPGA_GPIO[73]	F13	FPGA_GPIO[116]	AJ27
FPGA_GPIO[74]	G12	FPGA_GPIO[117]	AK27
FPGA_GPIO[75]	G11	FPGA_GPIO[118]	AH27
FPGA_GPIO[76]	G10	FPGA_GPIO[119]	AH28
FPGA_GPIO[77]	G8	FPGA_GPIO[120]	AK28
FPGA_GPIO[78]	F11	FPGA_GPIO[121]	AK29
FPGA_GPIO[79]	F10	FPGA_GPIO[122]	AH29
FPGA_GPIO[80]	E9	FPGA_GPIO[123]	AH30
FPGA_GPIO[81]	E8	FPGA_GPIO[124]	AG30
FPGA_GPIO[82]	E3	FPGA_GPIO[125]	AF30
FPGA_GPIO[83]	E4	FPGA_GPIO[126]	AH19
FPGA_GPIO[84]	AG22	FPGA_GPIO[127]	AH20
FPGA_GPIO[85]	AH22	FPGA_GPIO[128]	AF20
FPGA_GPIO[86]	AG23	FPGA_GPIO[129]	AG20
FPGA_GPIO[87]	AH23	FPGA_GPIO[130]	AK18
FPGA_GPIO[88]	AE19	FPGA_GPIO[131]	AK19
FPGA_GPIO[89]	AD17	FPGA_GPIO[132]	AJ19
FPGA_GPIO[90]	AH24	FPGA_GPIO[133]	AJ20
FPGA_GPIO[91]	AF24	FPGA_GPIO[134]	AK21

Signal name	Cyclone V Pin	Signal name	Cyclone V Pin
GPIO		GPIO	
FPGA_GPIO[135]	AJ21	FPGA_GPIO[152]	AA18
FPGA_GPIO[136]	AK22	FPGA_GPIO[153]	W17
FPGA_GPIO[137]	AJ22	FPGA_GPIO[154]	Y18
FPGA_GPIO[138]	AG21	FPGA_GPIO[155]	W19
FPGA_GPIO[139]	AE18	FPGA_GPIO[156]	V16
FPGA_GPIO[140]	AF21	FPGA_GPIO[157]	V17
FPGA_GPIO[141]	AE23	HPS_GPIO[0]	B26
FPGA_GPIO[142]	AC18	HPS_GPIO[1]	B25
FPGA_GPIO[143]	AA16	HPS_GPIO[2]	A25
FPGA_GPIO[144]	AC20	HPS_GPIO[3]	C25
FPGA_GPIO[145]	AG26	HPS_GPIO[4]	H20
FPGA_GPIO[146]	AF26	HPS_GPIO[5]	B23
FPGA_GPIO[147]	AB17	HPS_GPIO[6]	G22
FPGA_GPIO[148]	Y16	HPS_GPIO[7]	B22
FPGA_GPIO[149]	AA19	UART	
FPGA_GPIO[150]	W16	HPS_UART_RX	C23
FPGA_GPIO[151]	Y17	HPS_UART_TX	D22

Figure 33 : FPGA Connection Summary

Start Using ZEKE

Power Up ZEKE Board

Firstly, plug the power supply in to CN10, and see the power LEDs on the ZEKE board. LD1 for 5V and LD12 for 3.3V should be bright. The Figure 34 shows the location of power connector, power on LED, and power test points.

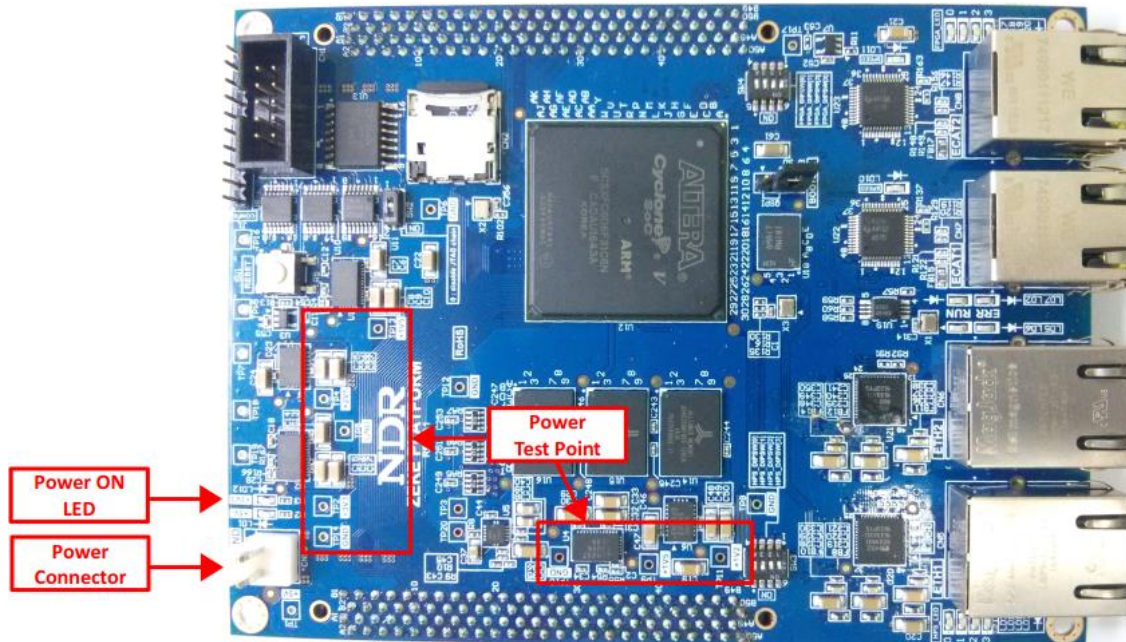


Figure 34 : Location of ZEKE Power

Step of Creating HPS on QSYS

1. Open Quartus Prime. Click at Tools -> QSYS as shown in the Figure 35.

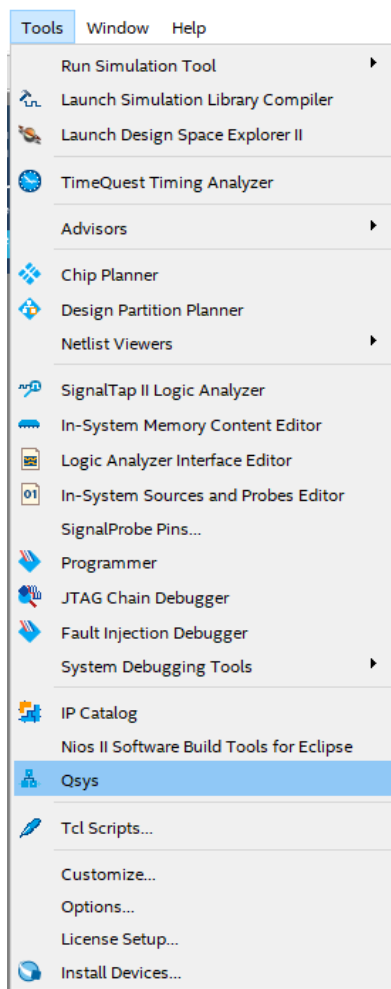


Figure 35 : QSYS Menu

2. On IP Catalog tab, search the word “hps”, then Arria V/Cyclone V Hard Processor System will appear as shown in the Figure 36. Double click it.

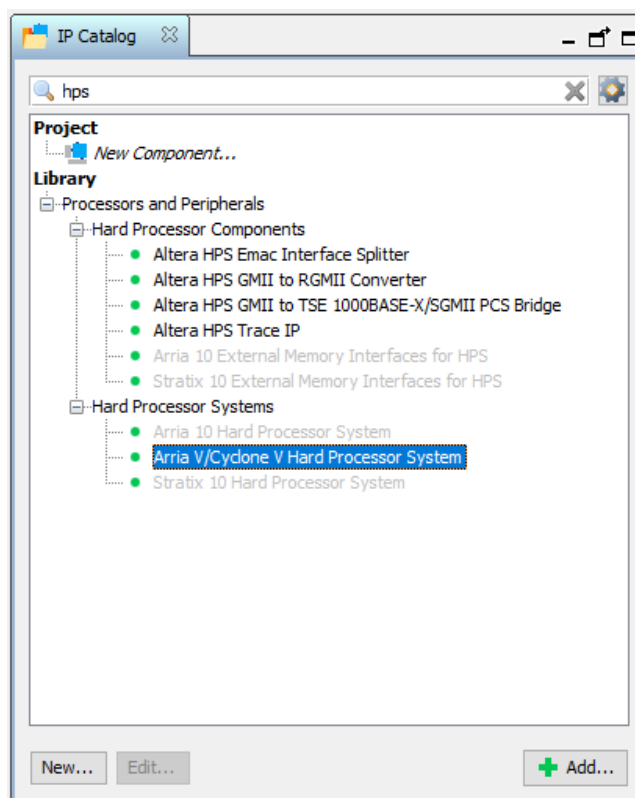


Figure 36 : HPS on IP Catalog

3. The default tab is FPGA Interfaces as shown in the Figure 37. Click the box according to the design.

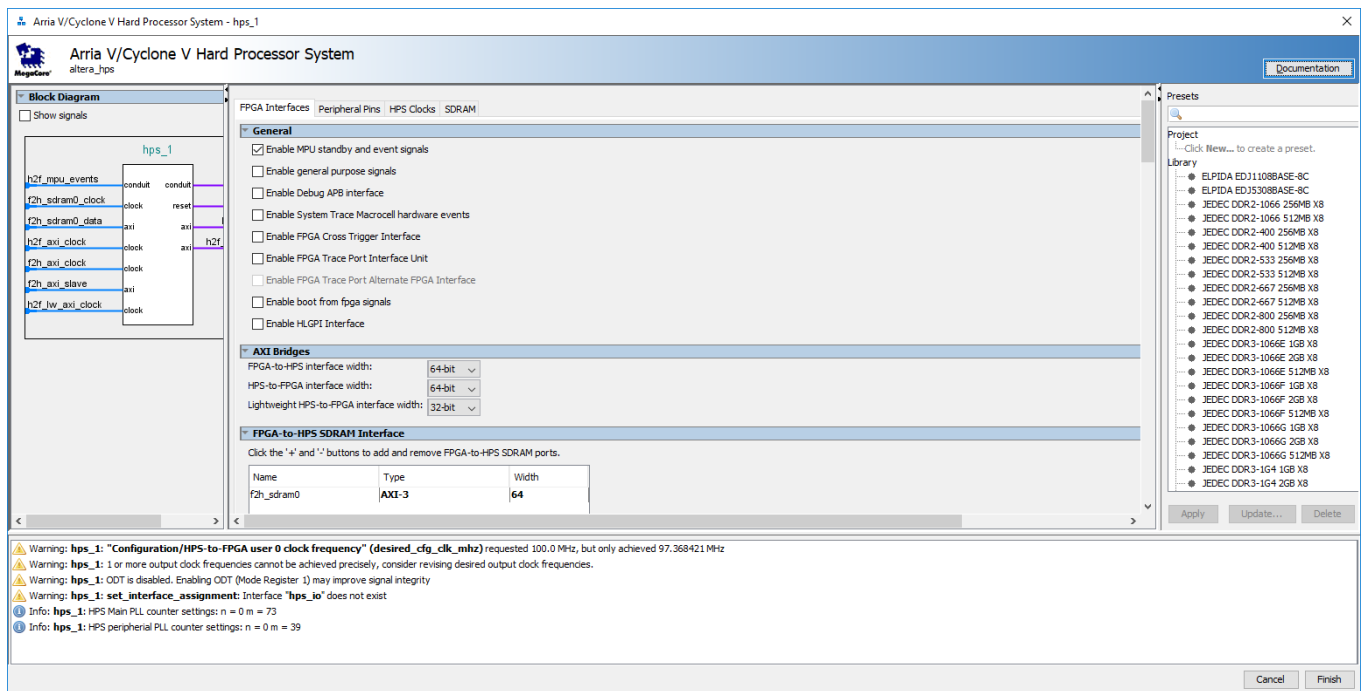


Figure 37 : Arria V/Cyclone V Hard Processor System

4. On Peripheral Pins tab, set the function pin and mode that is used in the design as shown in the Figure 38.

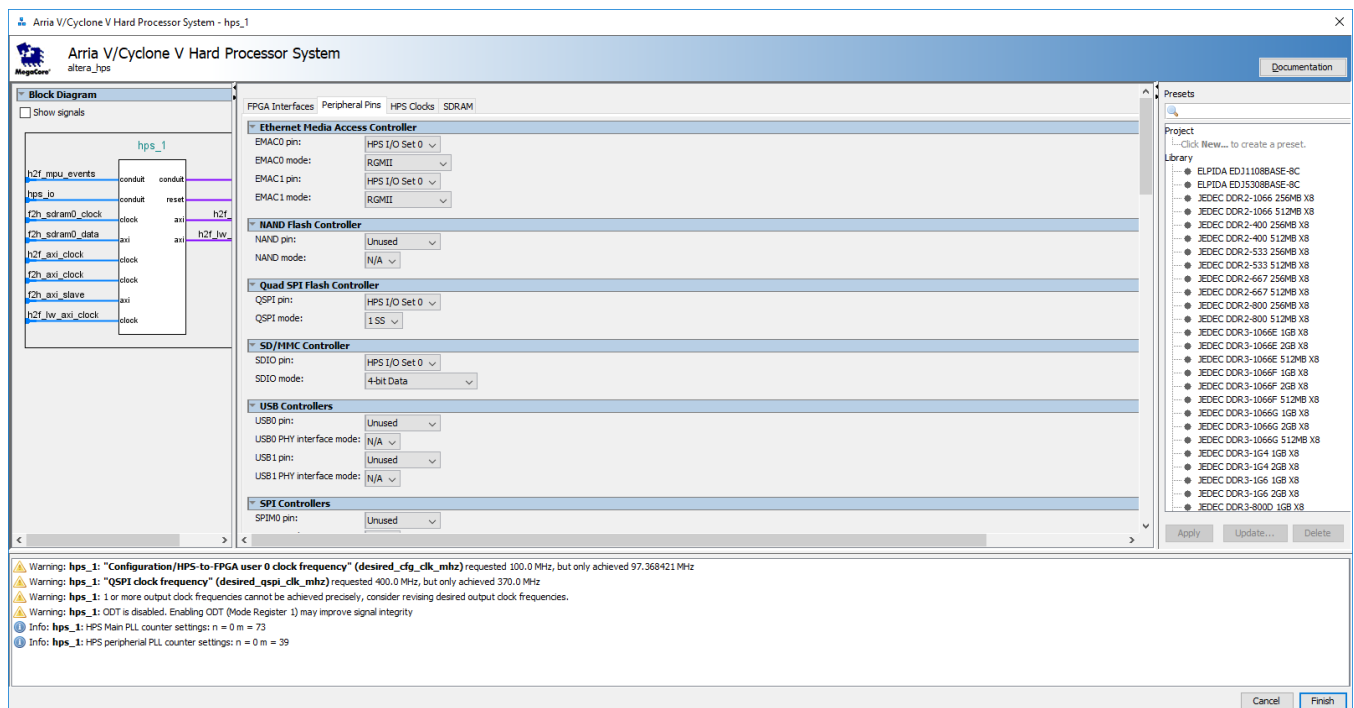


Figure 38 : Peripheral Pins of HPS

5. On SDRAM tab, select DDR3 in the box of SDRAM protocol, and the other parameters as shown in the

Figure 39. Then, click finish.

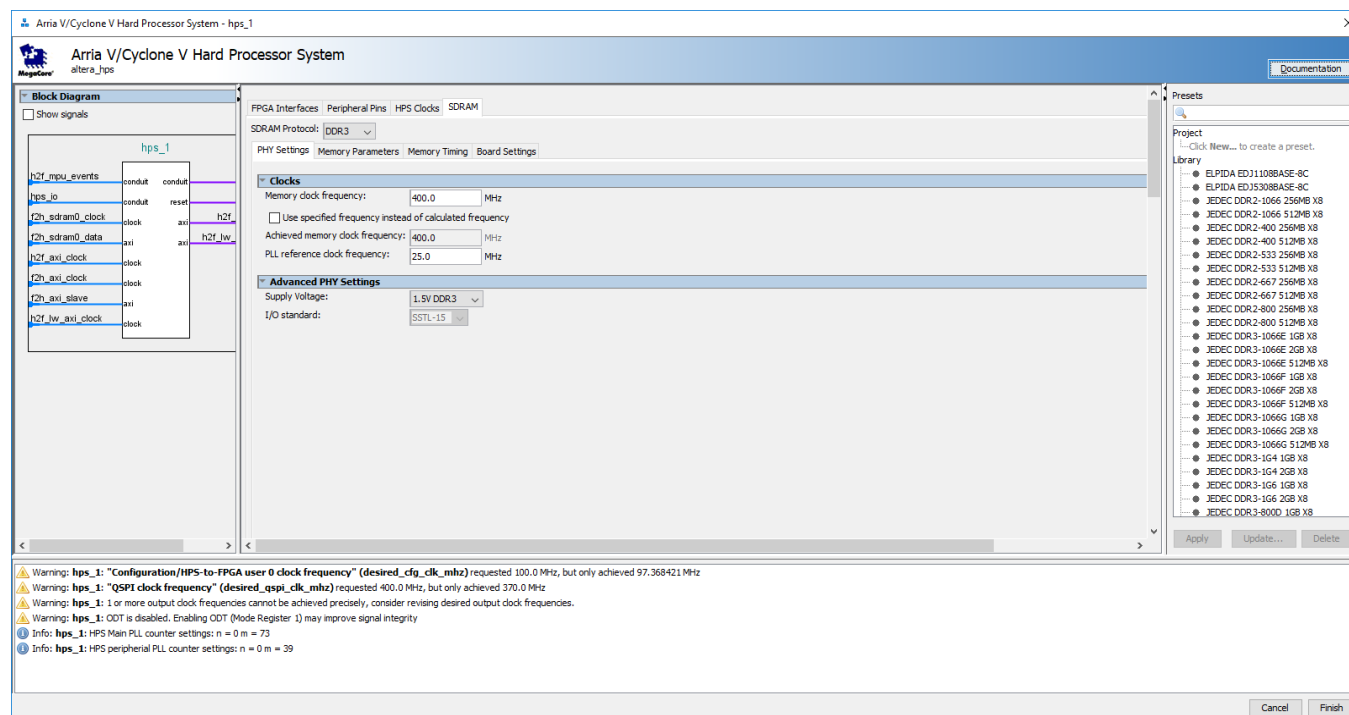


Figure 39 : SDRAM of HPS

6. Do the connection and address mapping of the design. Save the file if you have finished.

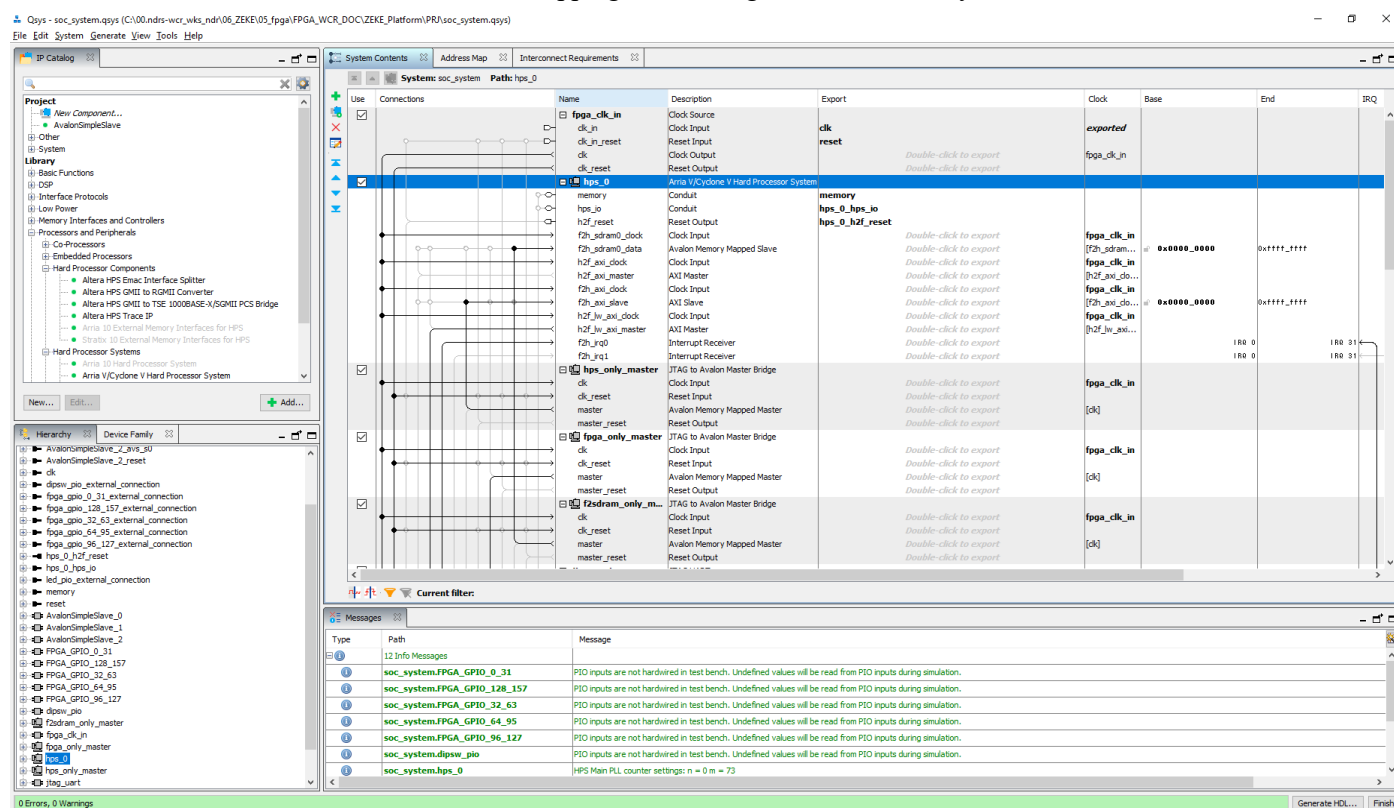


Figure 40 : HPS Design on QSYS

- Click **Generate HDL**. The windows in the Figure 41 will appear. Select the format file in Verilog or VHDL,

and then click Generate.

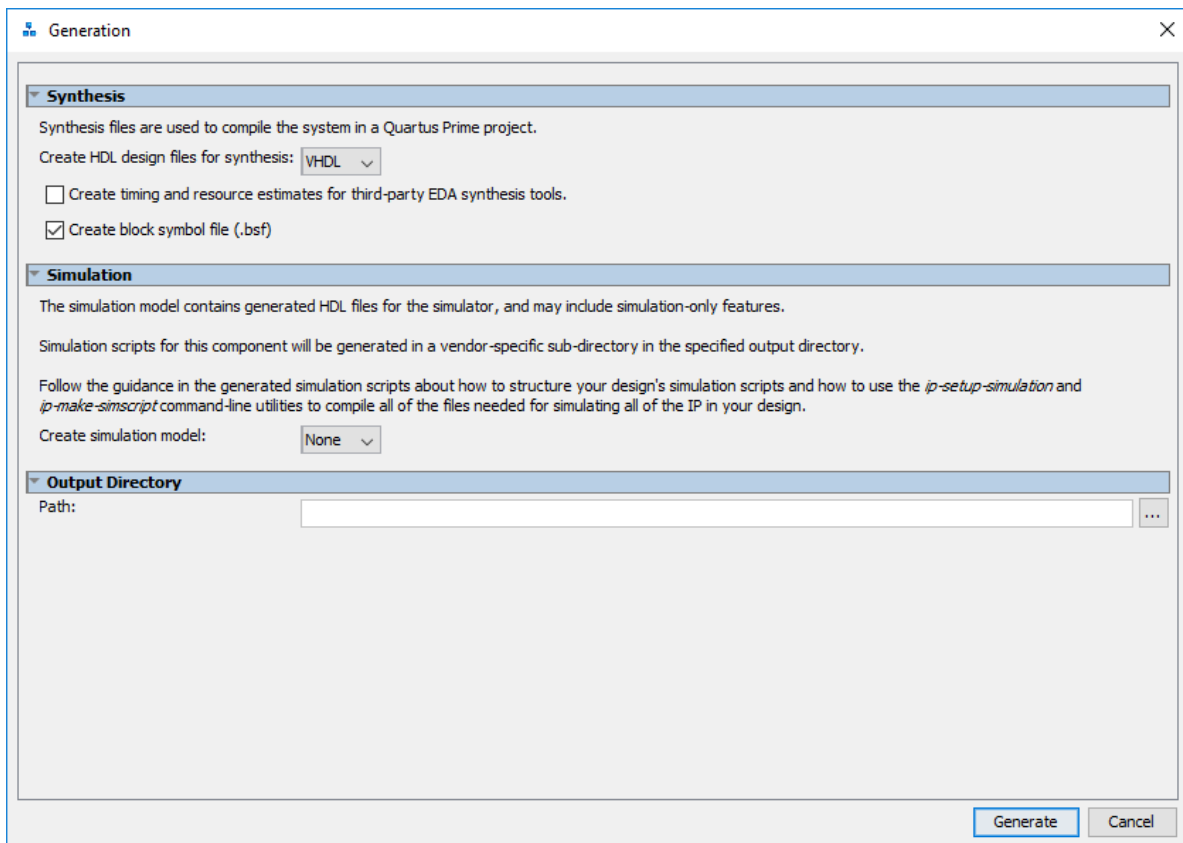


Figure 41 : QSYS Generate File

Step of Gerenerating SOF File

1. After you have finished creating HPS on QSYS, and TOP File of your design. Open Quartus Prime. Go to Assignment -> Settings as shown in the Figure 42.

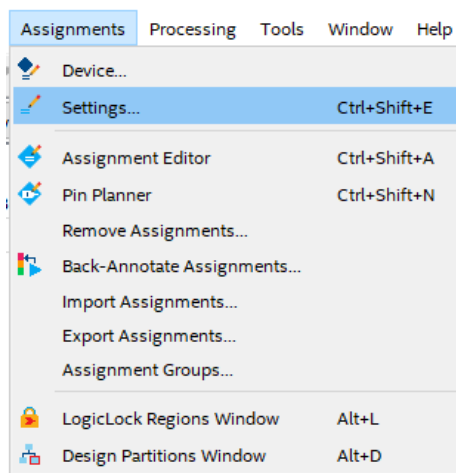


Figure 42 : Settings Menu in Quartus Prime

2. In Category, click Files, and add files to your project (QSYS file and/or TOP File). Then, click OK.

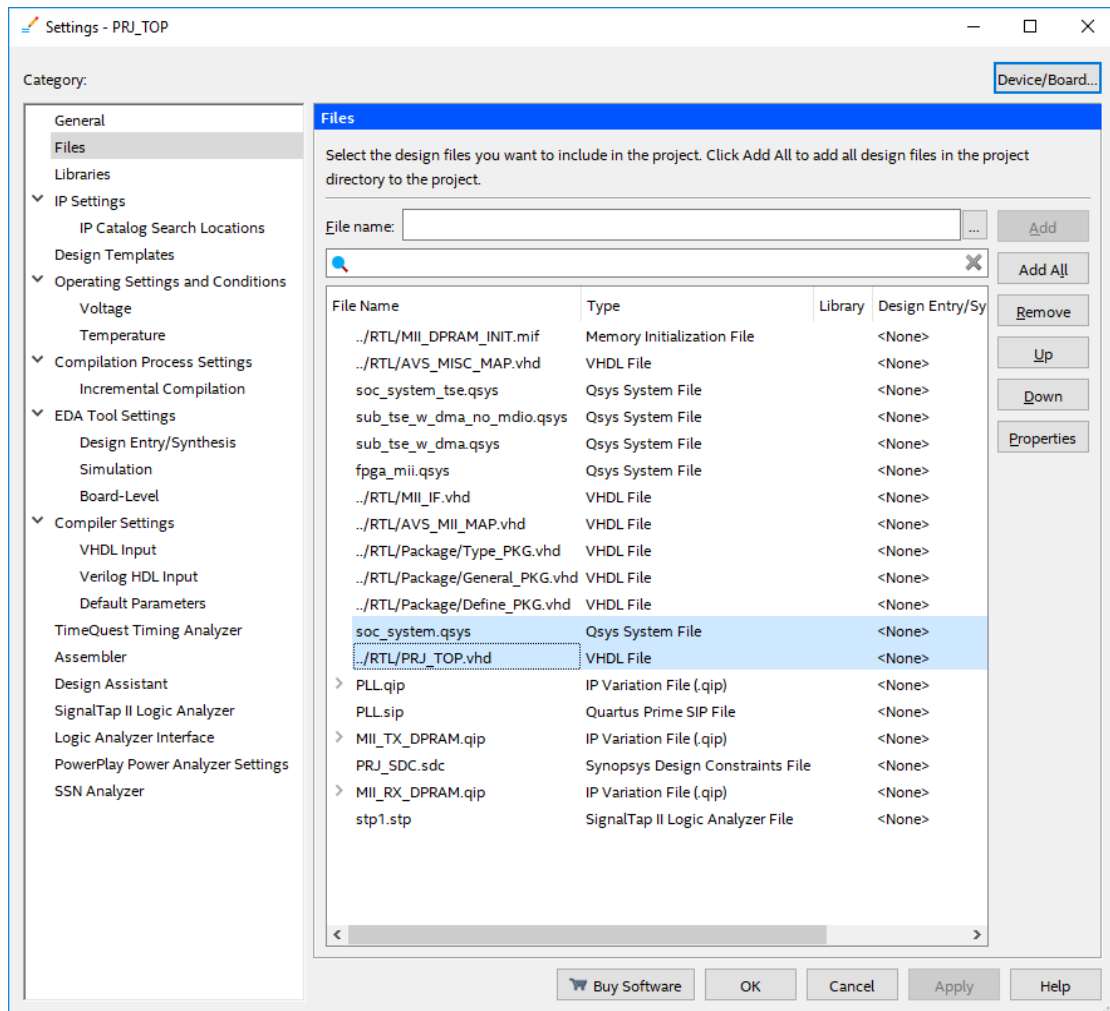


Figure 43 : Add File to Project

- Click Processing -> Start Compilation to compile the project.

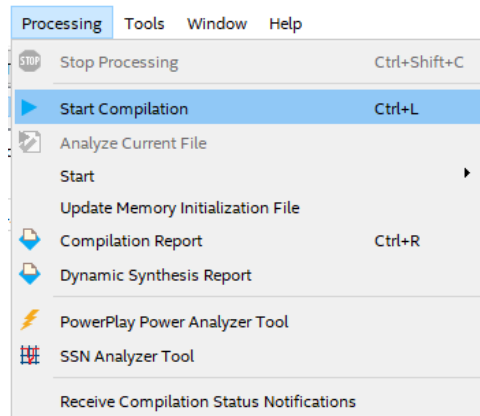


Figure 44 : Start Compilation

- After finished compiling the project, you will get SOF file in your output_files folder.

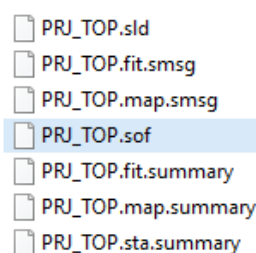


Figure 45 : SOF Output File

Step of Creating JIC File

1. Open Quartus Prime. Go to File -> Convert Programming Files as shown in the Figure 46.

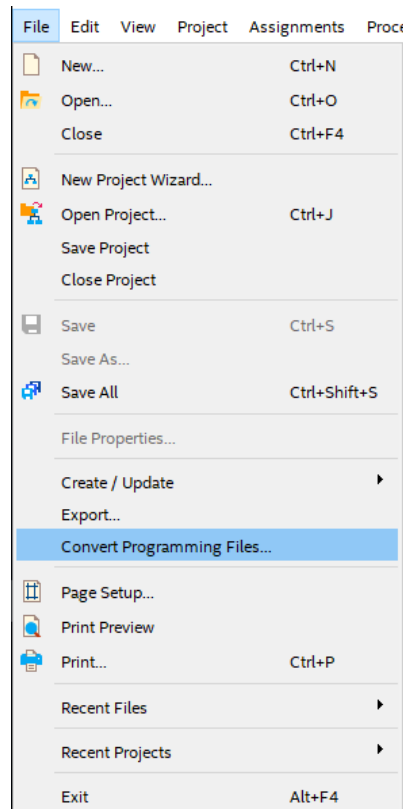


Figure 46 : Convet Programming Files Menu

2. Change Programming file type to JIC file as shown in the Figure 47.

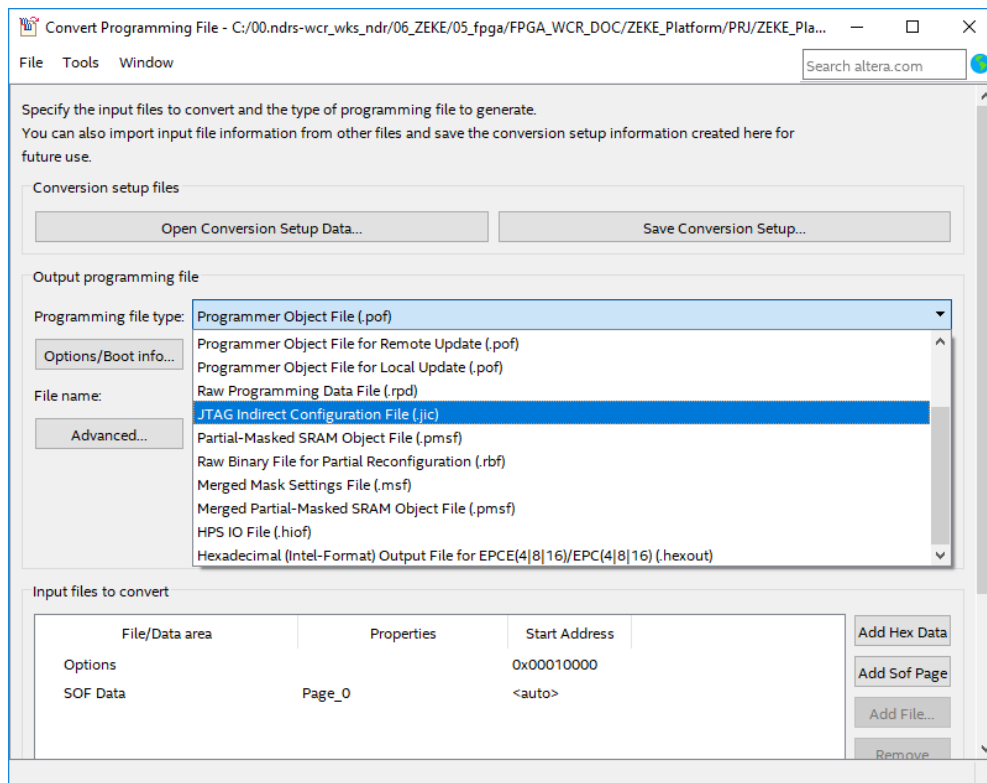


Figure 47 : Programming File Type

3. Select Configuration device. Select EPCQ64 for the ZEKE board, and then add Flash Loader and SOF Data by following the list below. Click Generate to get JIC file.

- Configuration device : EPCQ64
- Flash Loader : 5CSXFC6D6
- SOF Data : SOF file from compilation

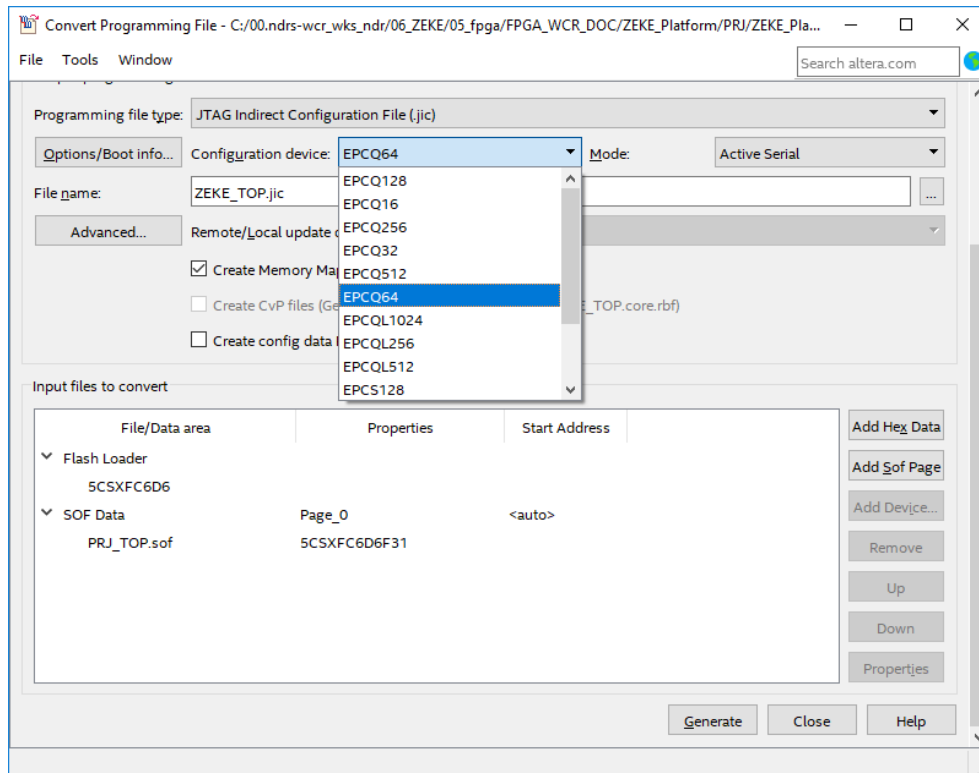


Figure 48 : Setting SOF File and Flash Loader

4. The JIC file is created in output_files folder.

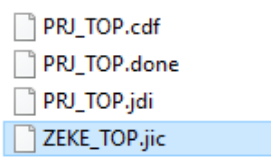


Figure 49 : JIC Output File

Step of Programming by JTAG

1. Open Quartus Prime. Click Tools -> Programmer to open programmer software.

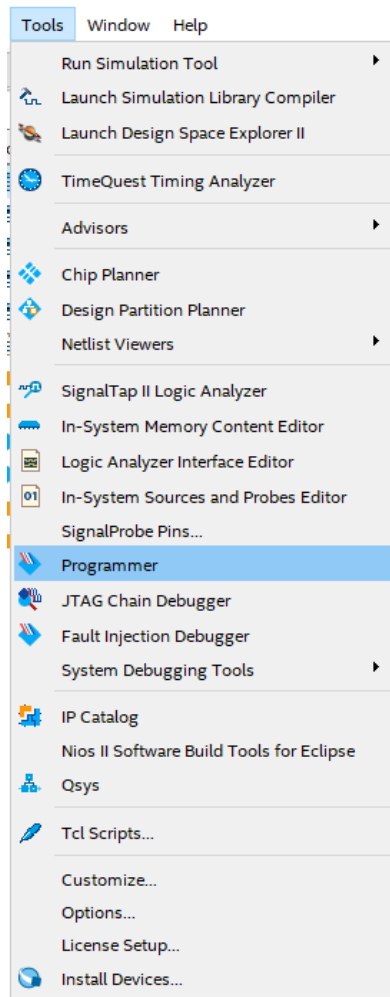


Figure 50 : Programmer Menu

2. Select Hardware Setup of progammer device.

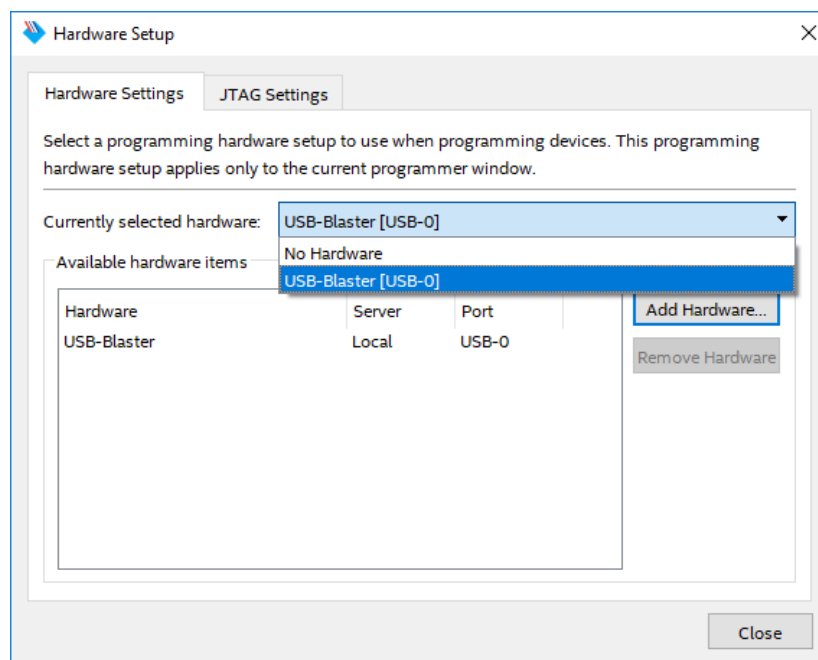


Figure 51 : Progeammer Device Setup

3. Add JIC file to the programmer. Check the box in Program/Configure column as shown in the Figure 52.

Make sure that SW2 is OFF (enable the JTAG chain), and then start to program.

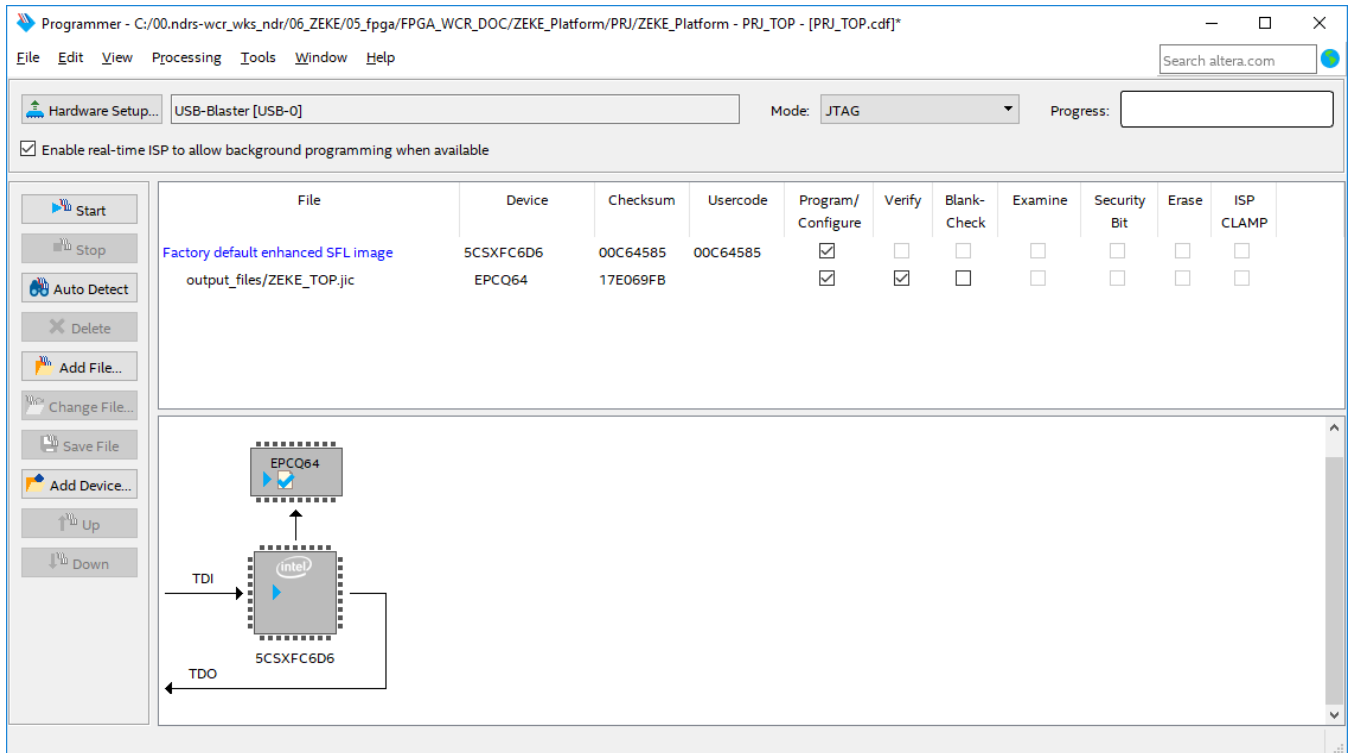


Figure 52 : Program the ZEKE board

Associated Product

OSCAR Board

The OSCAR board is an evaluation board which contains MAX 10, two of 10/100 Ethernet (PHY), SDRAM, EEPROM, NOR flash memory LED, rotary switch, and expansion connector. For more information please see on OSCAR Board User Manual. The look of the OSCAR board is shown in the Figure 53.

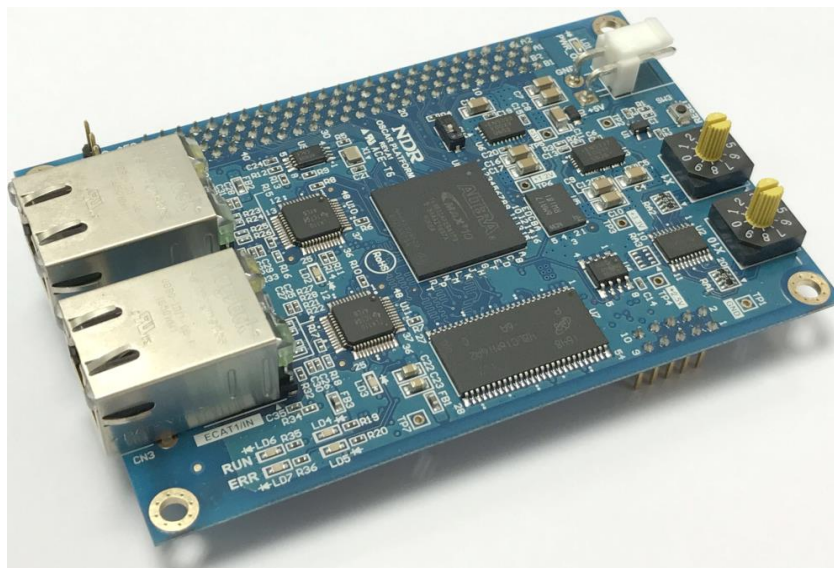


Figure 53 : OSCAR Board

Additional Information

Getting Help

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Revision History

Date	Revision	Changes list
2017-07-06	0.1	First draft
2017-10-05	0.2	Second draft (add more information)