

ZEKE-G Board User Manual

Revision 0.1

November 11, 2019

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Overview



Figure 1 : The ZEKE-G Board

ZEKE-G board is an evaluation board which contains Cyclone V System-on-Chip (SoC), DDR3 memory, four of 10/100/1000 Ethernet (PHY), four of USB 2.0 port, MicroSD Card connector, NOR flash memory along with user IO such as DIP switch, LED, and expansion connector.

The Cyclone V SoC has ARM Cortex A9 Hard Processor System (HPS) and FPGA separately in a single chip. Two of 10/100/1000 Ethernet (PHY) are implemented as Ethernet and two of 10/100/1000 Ethernet (PHY) are implemented as EtherCAT communication. User IO and expansion connector allow user to use ZEKE-G board to control the other device or board depending on user application.

MicroSD Card connector and NOR flash memory directly connect to HPS core which allow user to freely store application software or up to operating system (OS) for CPU to work accordingly.

Package Contents

- ZEKE-G Board RevA1.0
- ZEKE-G Board User Manual
- 5V DC Power Supply

Board Overview

The components on the ZEKE-G board are shown in the Figure below.

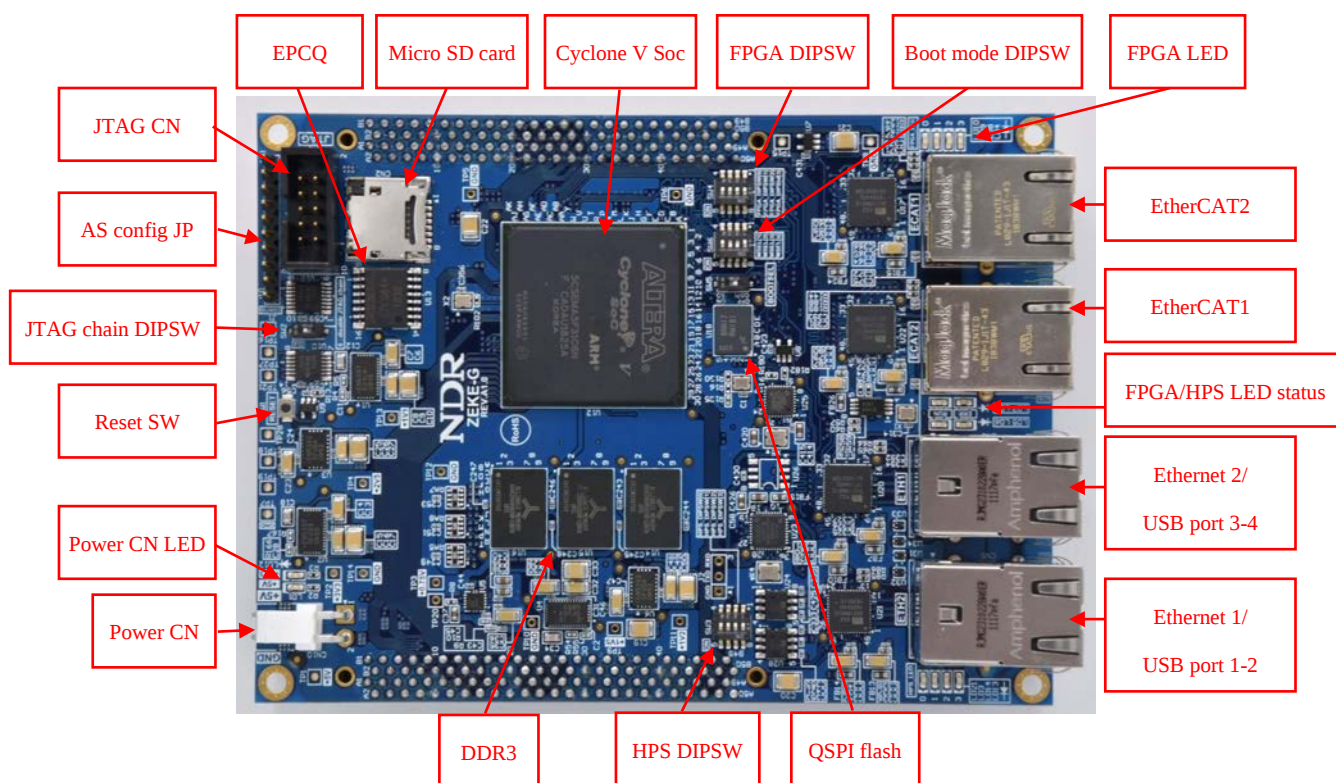


Figure 2 : Top View of ZEKE-G Board

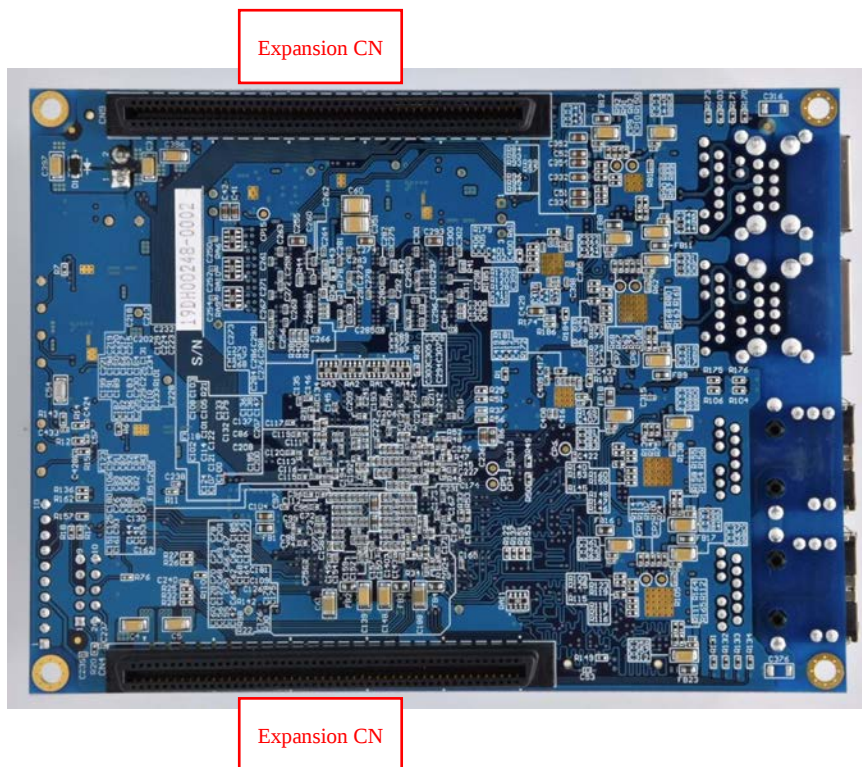


Figure 3 : Bottom View of ZEKE-G Board

Design Specification

- Power Connector : B2PS-VH(LF)(SN)
- FPGA : 5CSEMA5F31C6N (Cyclone V SoC)
- EPCQ : EPCQ64ASI16N (for FPGA)
- DDR3 x3 : 256Mb x 32 (+ ECC 8 bit)
- SD Card : MicroSD Card
- QSPI Flash : MT25QL512ABB8E12-0SIT (QSPI for HPS)
- Ethernet x2 : KSZ9031R (Connect to HPS RGMII) x 1,
KSZ9031M (Connect to HPS GMII) x 1
- EtherCAT x2 : KSZ9031M (Connect to FPGA)
- USB x4 : USB3300(USB PHY) + USB2514(USB Hub)
- LED : IO LED x8, Status LED x6, Power LED x2
- FPGA config mode switch : 4 bit switch x1
- HPS boot mode switch : 1 bit switch x1
- JTAG chain mode switch : 1 bit switch x1
- User DIP Switch : 4 bit switch x2
- Reset Switch : button switch x 1
- Expansion IO x2 : FX2C-100S-1.27DSA
(FPGA IO + HPS IO + UART + Power)

Block Diagram

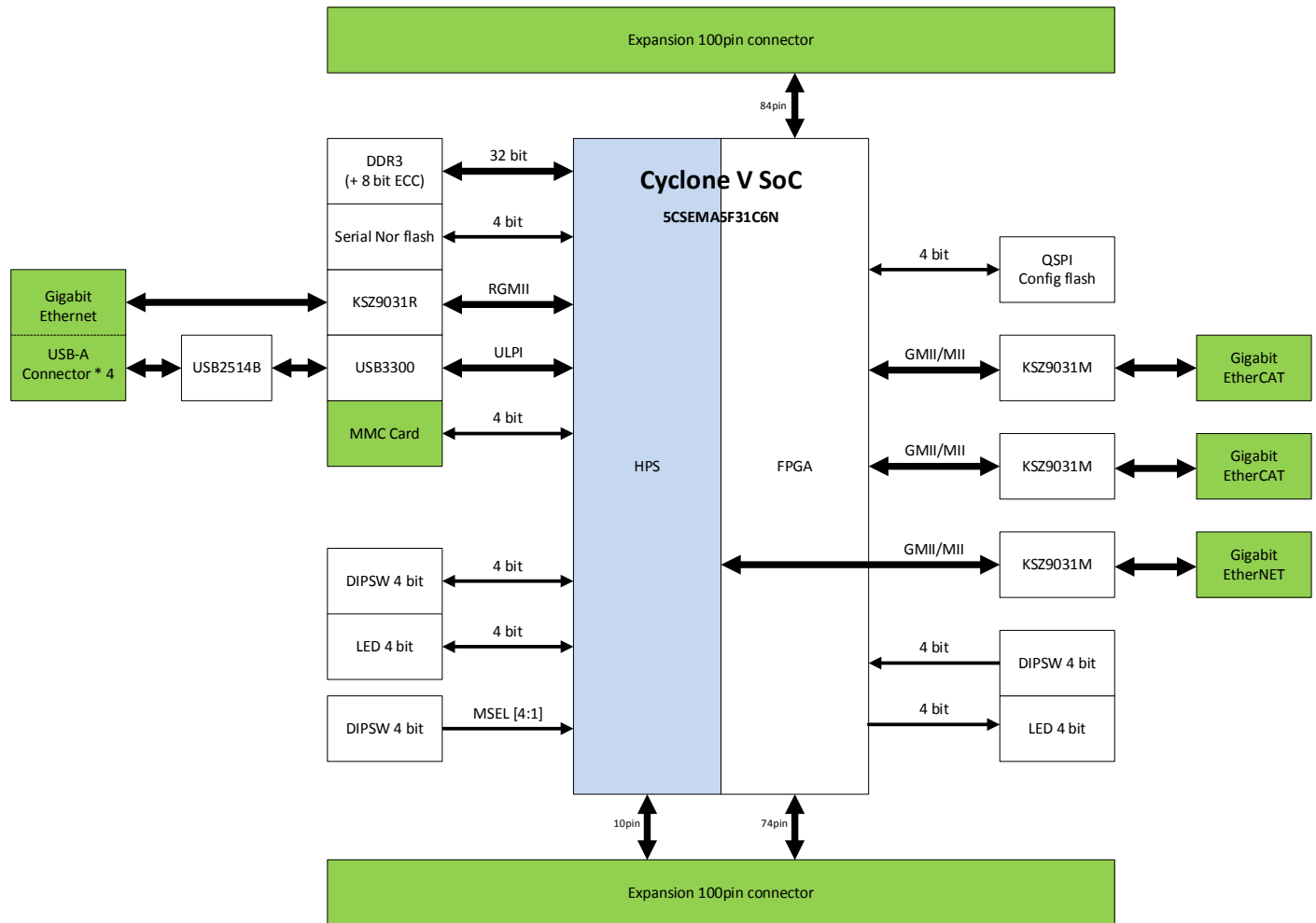


Figure 4 : Block Diagram

Power Supply

The ZEKE-G board is applied 5V power supply that recommend using at least 2A (output current of power supply). The connector of the power input is a 2-position header connector (CN10), and the part number is B2PS-VH(LF)(SN). After plug the power supply in, the power LEDs (LD1 and LD12), that is beside of power connector, should be bright.

Power Management

The ZEKE-G board is applied 5V power supply and generates voltage for the other components on the board. The DCDC converters and LDO regulator are used to regulate input voltage 5V to voltage level 0.75V, 1.1V, 1.2V, 1.5V, 2.5V, and 3.3V. There is the power sequence of the board. Firstly, 5V supplies to DCDC converter 1.1V, and then the DCDC converter generates 1.1V with Power OK (POK) signal. The POK is used to enable the other DCDC converters to generate the other voltage levels. The Figure 5 shows the power management structure. The Figure 6 shows the power sequence in timing diagram.

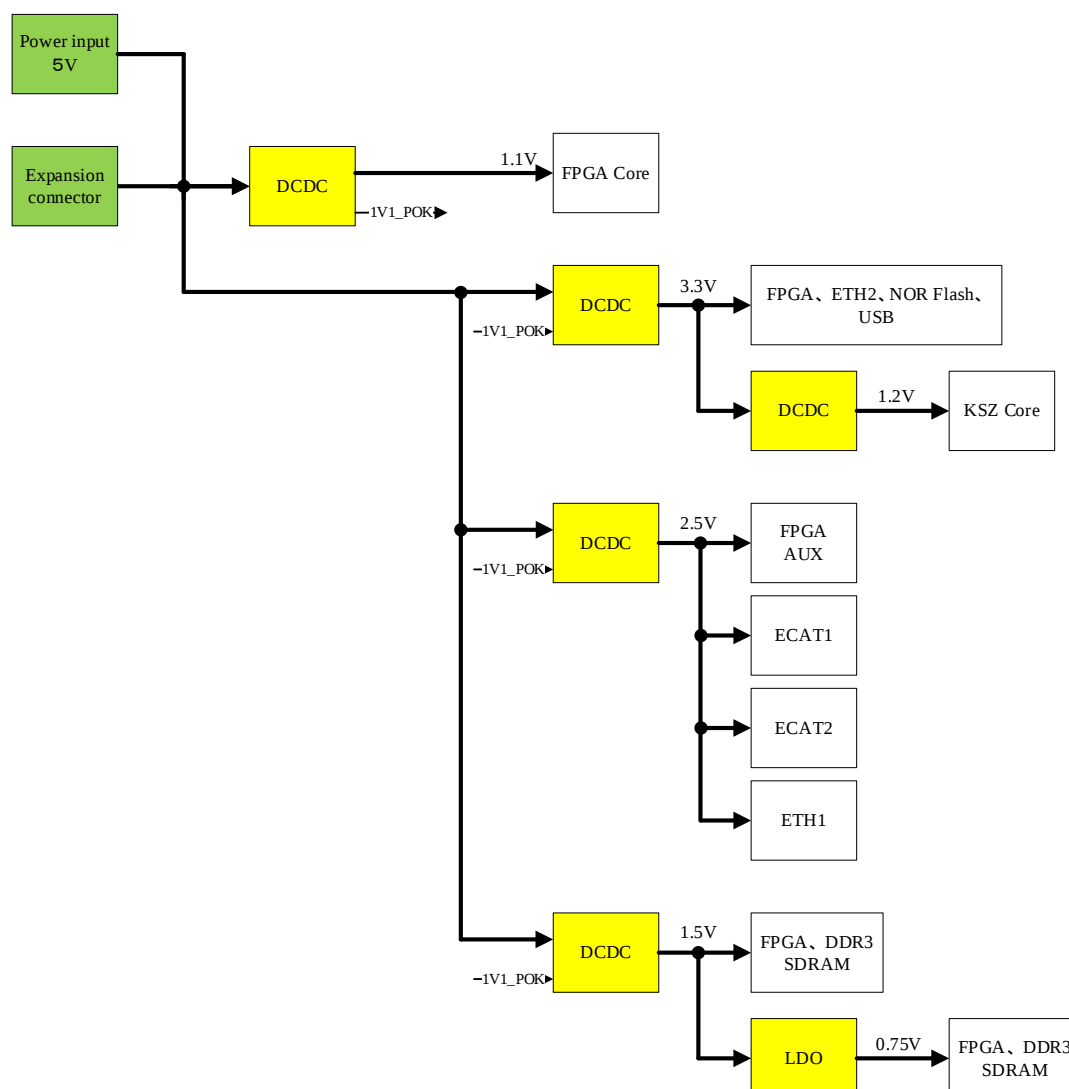


Figure 5 : Power Block Diagram

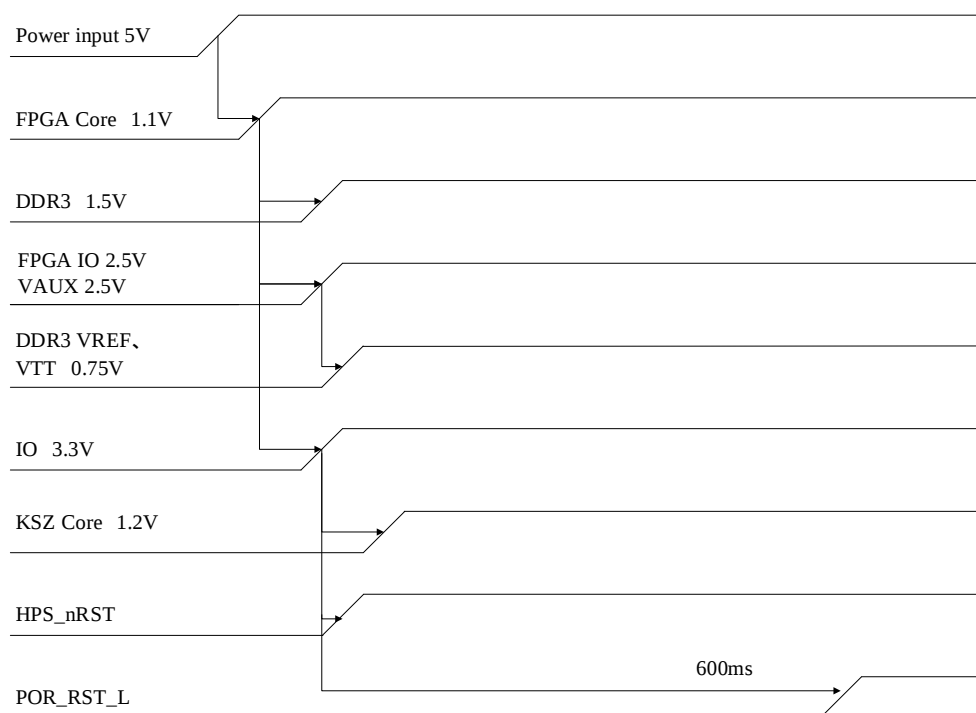


Figure 6 : Power Sequence Diagram

The ZEKE-G board uses Cyclone V SoC (5CSEMA5F31C6N) to be the main controller. This Cyclone V SoC has Hard Processor System (HPS) with ARM Cortex A9.

FPGA Power

The voltage level of Cyclone V SoC is designed in each bank following by the list below.

- Bank 3, 4, 5A and 7 : 3.3V
- Bank 5B and 8 : 2.5V
- Bank 6 : 1.5V (This bank is designed to control DDR and HPS DIP Switch)

FPGA Configutration

- nCONFIG = '1' : Normally no hard reset
- nCE = '0' : Normally always enable the chip
- MSEL[4..0] = FPGA configuration setting (setting by DIP switch)
- DEV_CLR = Not connected : Not using clear register function.
- DEV_OE = Not connected : Not using default IO state.
- BOOTSEL[2..0] = "1-1" : Boot from QSPI by set SW5 to OFF ("111") and SD card by set SW5 to ON ("101")
- CLKSEL[1..0] = "00" : Boot clock from osc1_clk / 4.

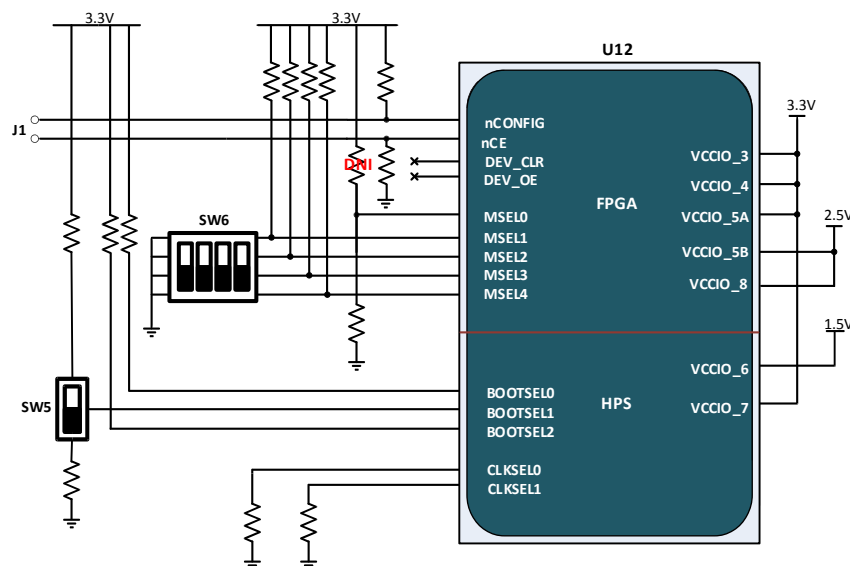


Figure 7 : FPGA Configuration

Note : Do Not Install (DNI) means that this part is not mounted for default.

JTAG

To program FPGA and HPS, you can program via JTAG connector (CN1) by enable JTAG chain on SW2 as shown in the Figure 8. To enable or disable JTAG chain, use SW2 by switching to OFF for enable and ON for disable.

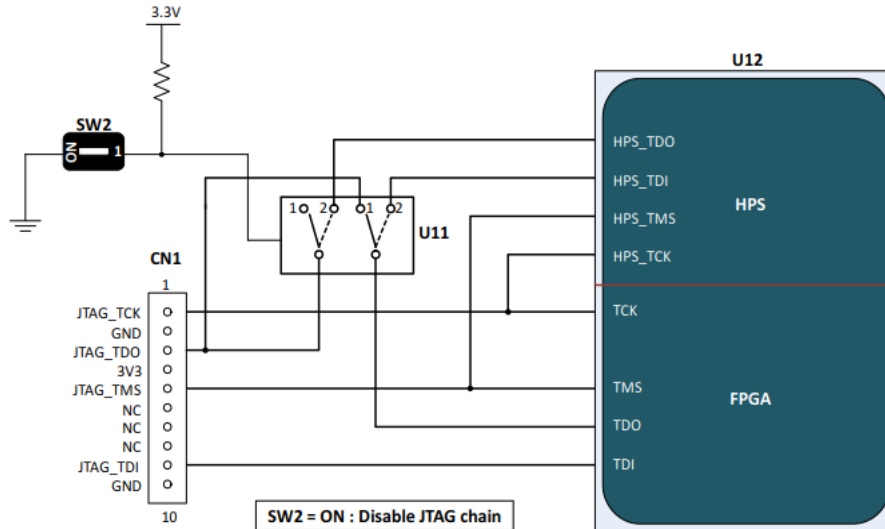


Figure 8 : JTAG Connection

Mode Setting

The mode setting on the ZEKE-G board has two type of setting mode, that are, configuration scheme (MSEL[4..0]) on FPGA and boot configuration on HPS as shown in the Figure 9.

For FPGA side, user can set FPGA configuration at DIP switch (SW6). By default MSEL[0] is set to '0', thus the variation of FPGA configuration setting is shown in Table 1.

For HPS side, the boot configuration is divided to clock select field (CLKSEL[1..0]) and boot select field (BOOTSEL[2..0]). CLKSEL is clock selection for booting, and it is set to "00" that means the clock selection for booting is oscl_clk divided by 4. BOOTSEL is used to define the source of booting. BOOTSEL can be selected to "101" for booting from MicroSD Card and "111" for booting from QSPI flash. You can select BOOTSEL[1] by slide switch (SW5), and there are SD label and QSPI label beside SW5.

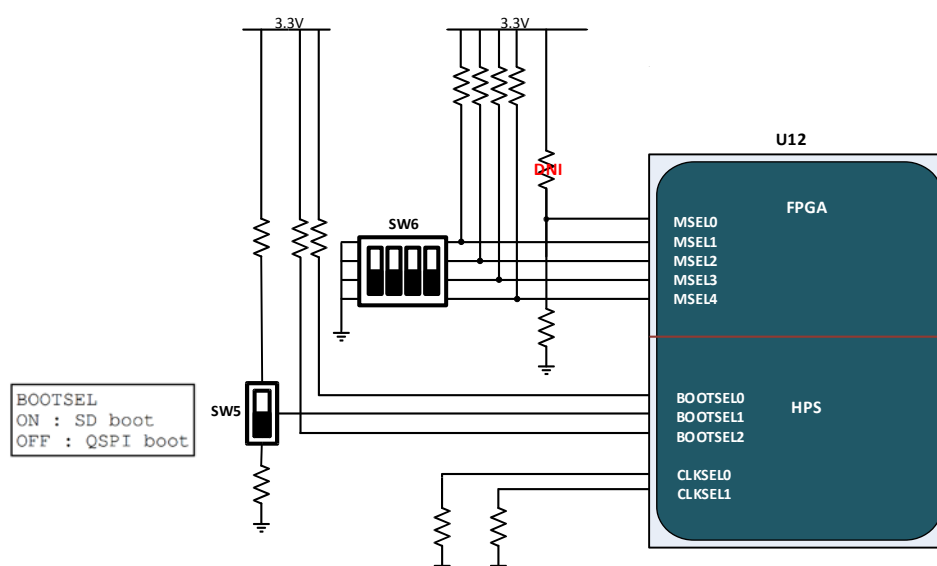


Figure 9 : Mode Setting Configuration

MSEL setting

Configuration Scheme	Compression Feature	POR delay	MSEL[4:0]
AS (x1 and x4)	_(1)	Fast	10010
FPP x8	Disabled	Fast	10100
	Disabled	Standard	11000
	Enabled	Fast	10110
	Enabled	Standard	11010
FPP x16	Disabled	Fast	00000
	Disabled	Standard	00100
	Enabled	Fast	00010
	Enabled	Standard	00110
FPP x32	Disabled	Fast	01000
	Disabled	Standard	01100
	Enabled	Fast	01010
	Enabled	Standard	01110

Table 1 : FPGA configuration setting (MSEL)

(1) Can enabled/disabled when generate bitstream file by Quartus software.

HPS boot mode	BOOTSEL[2:0]
HPS boot from SD/MMC flash	101
HPS boot from quad SPI flash	111

Table 2 : HPS boot setting (BOOTSEL)

Clock Source

The ZEKE-G board has three clock sources for FPGA, HPS, and four Ethernet PHY chips. All clock sources are the same part number (SG-210STF25.000000MHzL), and the frequency is 25MHz with 50 ppm. The clock source of Ethernet PHY chip uses clock buffer to drive each Ethernet PHY chip. USB controller and USB hub use 24MHz crystal oscillator. Figure 10 shows block diagram of clock sources.

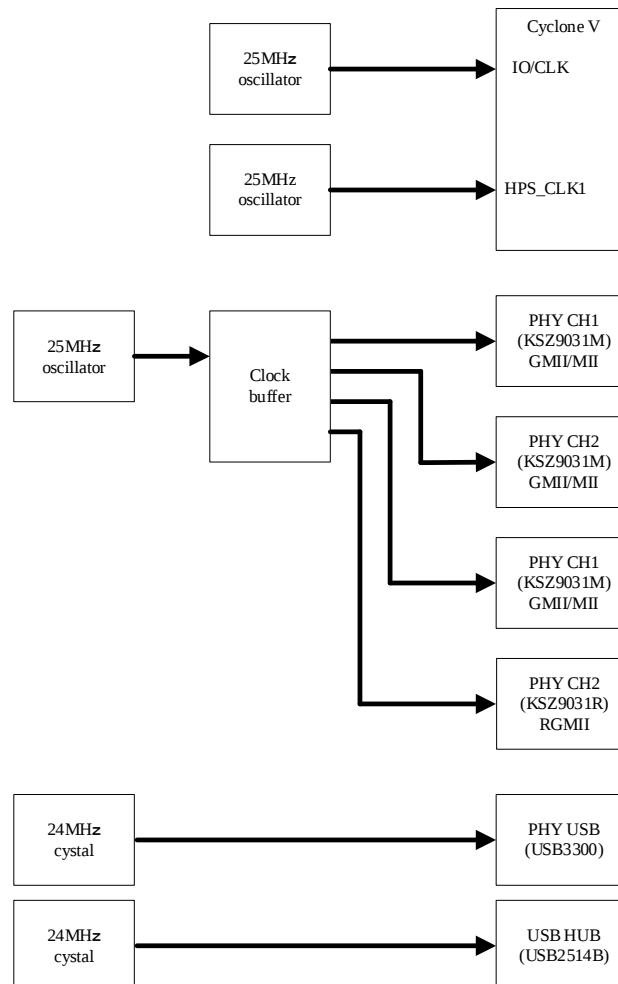


Figure 10 : Clock Source

Reset System

During power up all of devices will be reseted. After of all power stable, there will wait 600ms for FPGA configuration finish. Then HPS and FPGA will run in user mode. All of devices will release from reset state. The Gigabit EtherCAT PHY reset pin will be controlled by FPGA. ZEKE-G all also prepare reset switch (SW1). When SW1 is pushed, all of devices will be reseted. Figure 11 shows block diagram of reset system. Figure 12 shows reset timing.

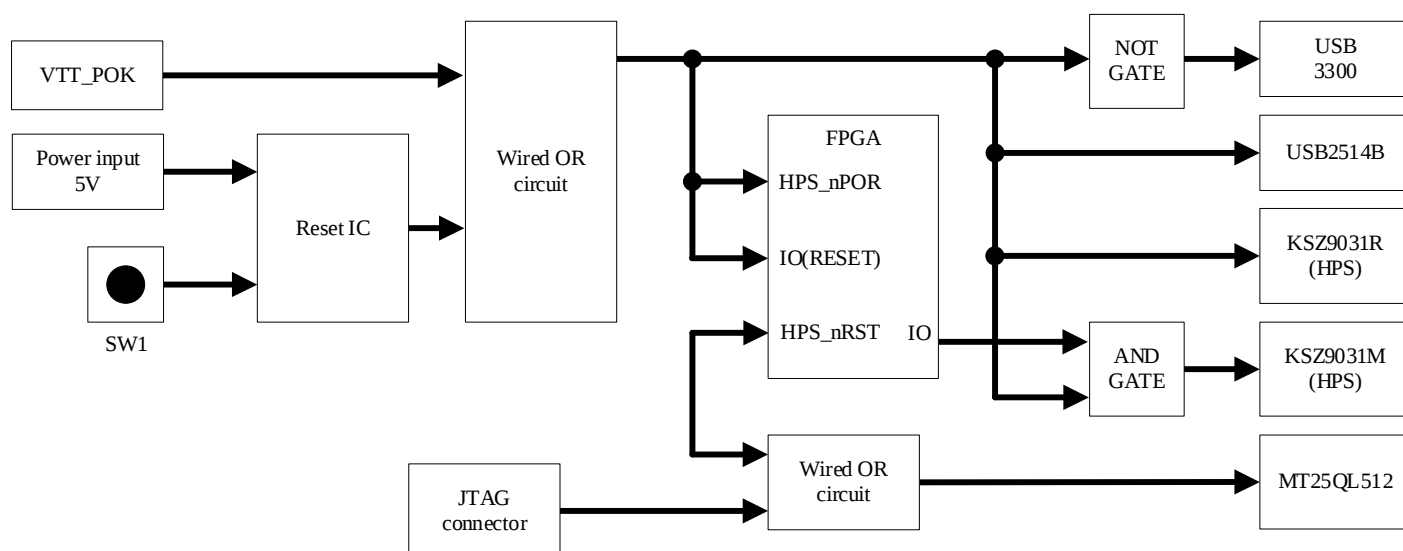


Figure 11 : Reset System

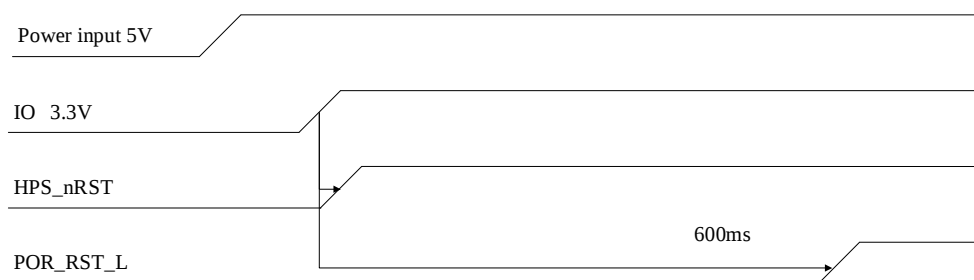


Figure 12 : Example of Resetting by FPGA_CONF_DONE

Quad-Serial Configuration (EPCQ) 64Mbit is a non-volatile memory, and used to save the configuration file on FPGA side. The part number is EPCQ64ASI16N. The ZEKE-G board is designed to program EPCQ by three ways, that are, indirect programming, direct programming, and Linux programming.

Indirect Programming

The indirect programming uses JTAG interface. To program this way, you have to connect USB Blaster to JTAG connector (CN1) as shown in Figure 13, and enable the JTAG chain by switching SW2 to OFF.

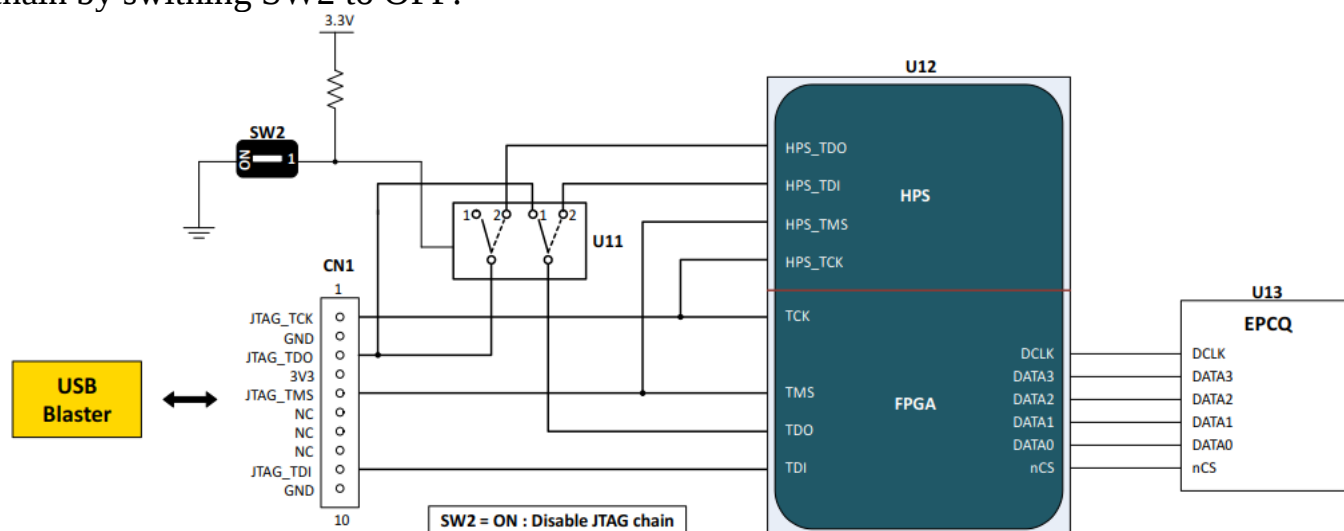


Figure 13 : Indirect Programming

Direct Programming

The direct programming uses the Active-Serial (AS) interface. Connect USB Blaster to header connector (J1) to program as shown in Figure 14.

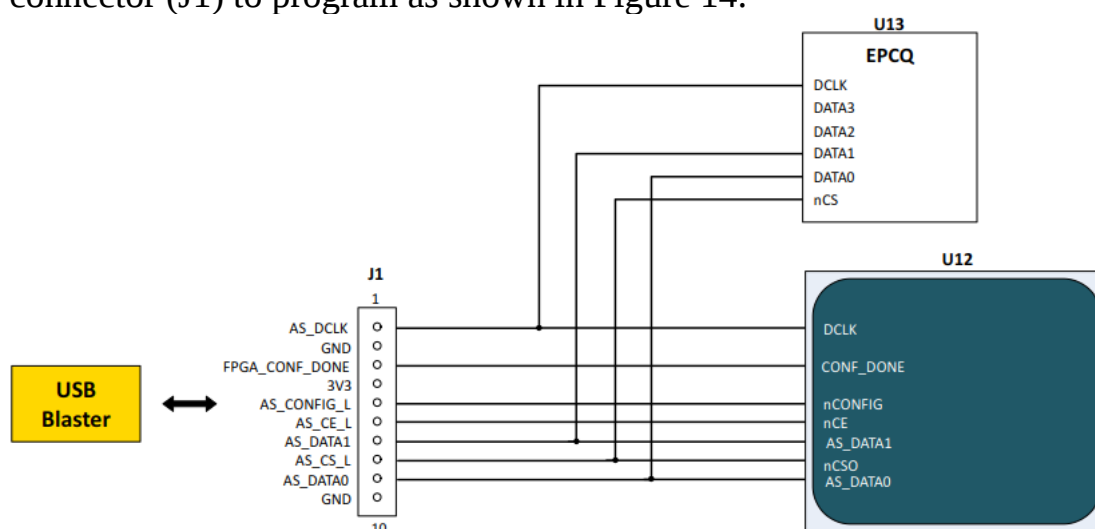


Figure 14 : Direct Programming

Linux Programming

The Linux programming is programming method that can program EPCQ by using MicroSD Card. Slot the MicroSD Card in to CN2, and then power up the ZEKE-G board. The EPCQ will be programmed by HPS.

DDR3

The ZEKE-G board includes three DDR3s 4Gb (256M x 16). The two of DDR3s are designed to be a simple RAM, and the another one is designed to be an Error-Correction Code memory (ECC memory). The total capacity of the memory is 8Gb (256M x 32). The DDR3s are connected to the hard memory controller in the HPS. The DDR3s use voltage level 1.5V SSTL-compatible inputs, and the speed grade of DDR3s interface is DDR3-1600.

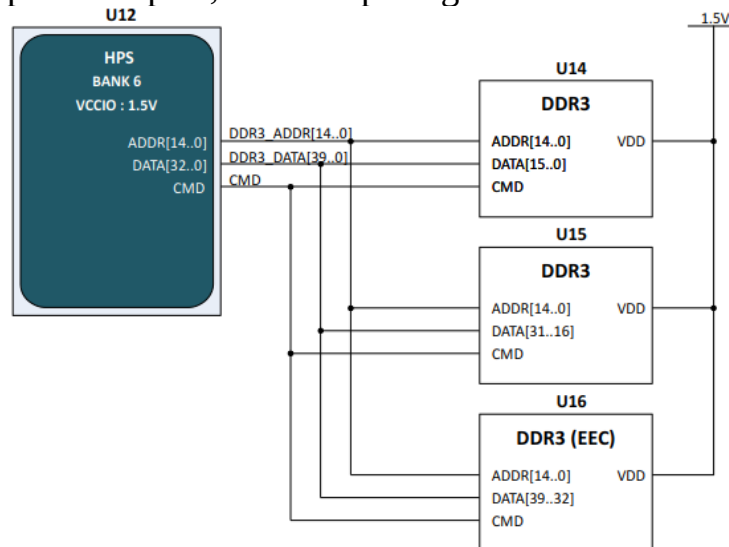


Figure 15 : DDR3

MicroSD Card

MicroSD Card slot (CN2) on the board is connected to HPS for booting Linux. The 4-bit data and the command of SD mode is used to access the MicroSD Card. To boot from MicroSD Card, slot the SD Card in, and set the mode selection for booting from MicroSD Card on SW5 (SW5 : ON).

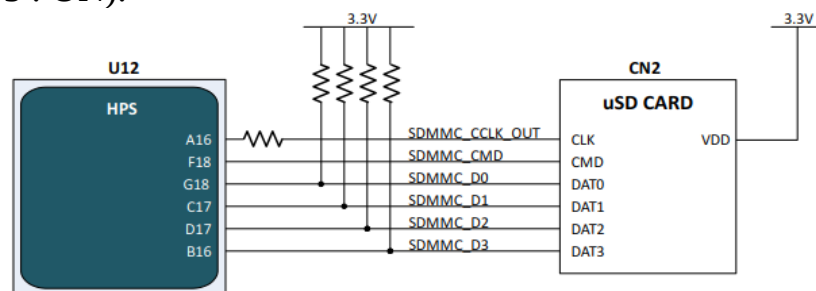


Figure 16 : MicroSD Card

QSPI Flash

On the HPS side, QSPI (MT25QL512ABB8E12-0SIT) 512Mbit is used to save the program file for booting HPS. The QSPI flash can be programmed by JTAG interface or MicroSD Card. To program the QSPI flash via JTAG interface, DON'T forget to switch the SW2 to OFF (enable JTAG chain) and select QSPI mode on SW5 (SW5 : OFF).

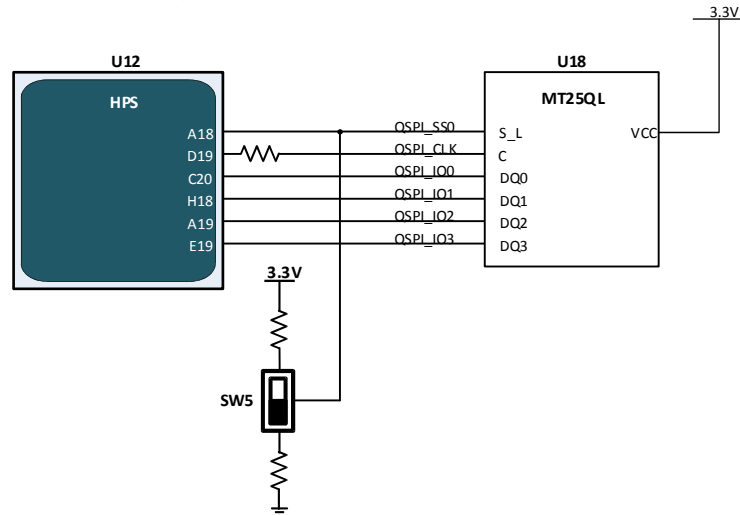


Figure 17 : QSPI Flash

Ethernet

ZEKE-G has 2 Gigabit Ethernet ports. One use KSZ9031RNXIC connected with RGMII interface. Another use KSZ9031MNXIC connected with GMII interface. Both are connected directly to HPS core (KSZ9031MNXIC is connected via FPGA IO pin). The Ethernet PHY support auto negotiation and auto MDI/MDI-X.

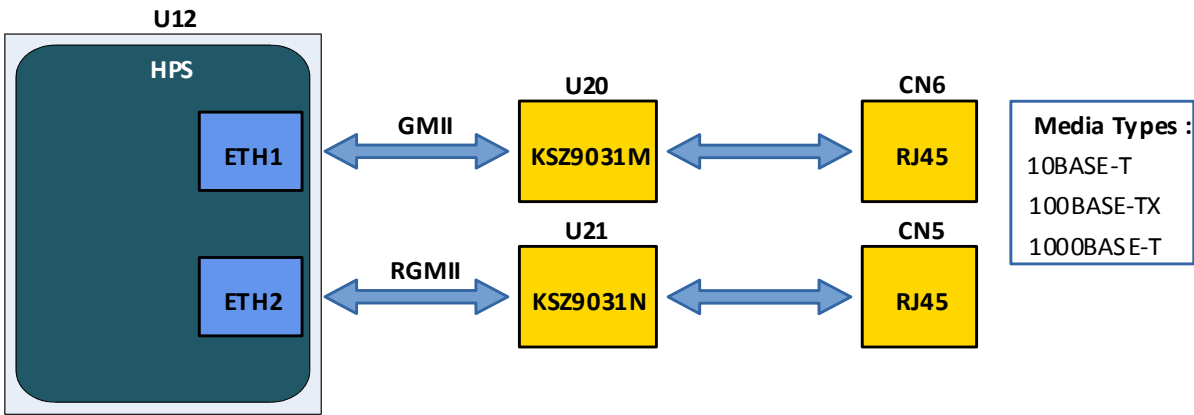


Figure 18 : Ethernet Connection

	Ethernet 1	Ethernet 2
PHYAD[4:0]	“00100”	“00110”

Table 3 : Ethernet Address

Ethernet 1	FPGA pin	Ethernet 2	FPGA pin
ETH1_INT_L	F6	HPS_ETH2_INT_L	C19
ETH1_MDC	G7	HPS_ETH2_MDC	B21
ETH1_MDIO	C13	HPS_ETH2_MDIO	E21
ETH1_RX_CLK	H15	HPS_ETH2_RX_CLK	G20
ETH1_RX_DV	J14	HPS_ETH2_RX_CTL	K17
ETH1_RX_ER	E4	HPS_ETH2_RXD[0]	A21
ETH1_RXD[0]	J10	HPS_ETH2_RXD[1]	B20
ETH1_RXD[1]	E7	HPS_ETH2_RXD[2]	B18
ETH1_RXD[2]	J9	HPS_ETH2_RXD[3]	D21
ETH1_RXD[3]	E6	HPS_ETH2_TX_CTL	A20
ETH1_RXD[4]	J7	HPS_ETH2_TXD[0]	F20
ETH1_RXD[5]	B7	HPS_ETH2_TXD[1]	J19
ETH1_RXD[6]	G11	HPS_ETH2_TXD[2]	F21
ETH1_RXD[7]	G15	HPS_ETH2_TXD[3]	F19
ETH1_TX_COL	F8	-	-
ETH1_TX_CRS	G10	-	-
ETH1_TX_EN	H7	-	-
ETH1_TX_ER	G12	-	-
ETH1_TXD[0]	J12	-	-
ETH1_TXD[1]	K7	-	-
ETH1_TXD[2]	E3	-	-
ETH1_TXD[3]	K8	-	-
ETH1_TXD[4]	E2	-	-
ETH1_TXD[5]	K12	-	-
ETH1_TXD[6]	E1	-	-
ETH1_TXD[7]	F10	-	-

Table 4 : Ethernet pin description

ZEKE-G has 2 Gigabit Ethernet ports that implement as EtherCAT communication. Both are connected to FPGA pin. The Ethernet PHY support auto negotiation, auto MDI/MDI-X. ZEKE-G is shipped with sample EtherCAT master.

In another hand, cause of KSZ9031MNXIC is only Gigabit ethernet PHY. Thus, user can implement KSZ9031MNXIC as any communction. Such as Ethernet TCP/IP, EtherCAT slave.

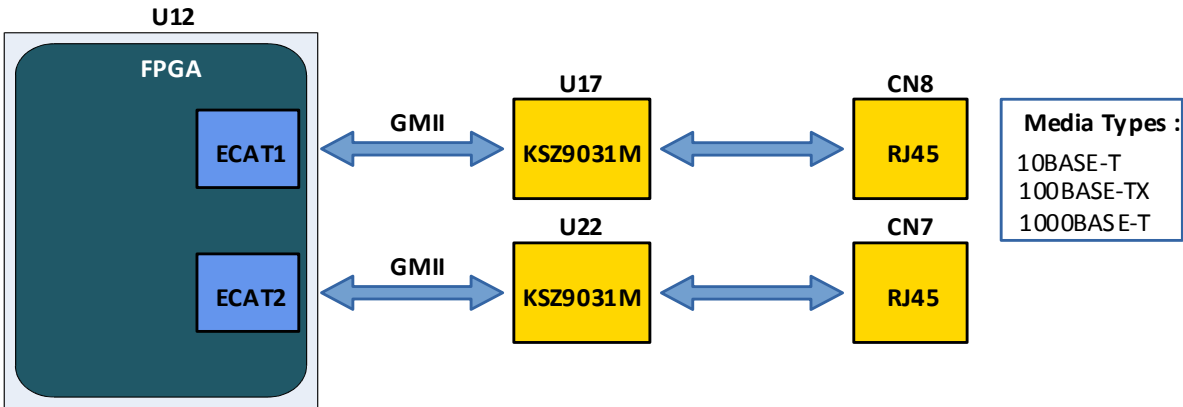


Figure 19 : EtherCAT Connection

	EtherCAT 1	EtherCAT 2
PHYAD[4:0]	“00001”	“00011”

Table 5 : EtherCAT Address

Ethernet 1	FPGA pin	Ethernet 2	FPGA pin
ECAT1_INT_L	E8	ECAT2_INT_L	E11
ECAT1_RX_CLK	AA26	ECAT2_RX_CLK	K14
ECAT1_RX_DV	B3	ECAT2_RX_DV	D11
ECAT1_RX_ER	B5	ECAT2_RX_ER	D12
ECAT1_RXD[0]	D4	ECAT2_RXD[0]	F13
ECAT1_RXD[1]	D2	ECAT2_RXD[1]	E13
ECAT1_RXD[2]	D1	ECAT2_RXD[2]	H8
ECAT1_RXD[3]	A13	ECAT2_RXD[3]	G8
ECAT1_RXD[4]	A9	ECAT2_RXD[4]	E12
ECAT1_RXD[5]	A8	ECAT2_RXD[5]	H13
ECAT1_RXD[6]	B13	ECAT2_RXD[6]	H12
ECAT1_RXD[7]	B11	ECAT2_RXD[7]	F11
ECAT1_TX_COL	A4	ECAT2_TX_COL	C9
ECAT1_TX_CRS	A3	ECAT2_TX_CRS	C8
ECAT1_TX_EN	A5	ECAT2_TX_EN	C10
ECAT1_TX_ER	B6	ECAT2_TX_ER	C7
ECAT1_TXD[0]	B2	ECAT2_TXD[0]	D10
ECAT1_TXD[1]	B1	ECAT2_TXD[1]	D9
ECAT1_TXD[2]	C5	ECAT2_TXD[2]	D7
ECAT1_TXD[3]	C4	ECAT2_TXD[3]	F15
ECAT1_TXD[4]	C3	ECAT2_TXD[4]	F14
ECAT1_TXD[5]	C2	ECAT2_TXD[5]	E9
ECAT1_TXD[6]	D6	ECAT2_TXD[6]	H14
ECAT1_TXD[7]	D5	ECAT2_TXD[7]	G13
ECAT1_ACTIVE	AD30	ECAT2_ACTIVE	AA30
ECAT1_LINK	AA28	ECAT2_LINK	AB28
ECAT1_LED1	AE9	ECAT2_LED1	AD12
ECAT1_LED2	AE7	ECAT2_LED2	AD14
ECAT1_LED3	AD7	ECAT2_LED3	AC12
Others	FPGA pin	Others	FPGA pin
PHY1_2_RESET_L	AB27	ECAT_MDC	B12
ECAT_LED_ERR	AB15	ECAT_MDIO	B8
ECAT_LED_RUN	AC14		

Table 6 : EtherCAT pin description

USB2.0

USB PHY chips (USB3300) is used to design on the ZEKE-G board to interface with USB communication. The USB2514B is used as a USB hub to expand USB port. ZEKE-G has USB 4 ports that output at CN5, CN6 connector (2 ports for each). ZEKE-G board use HPS USB controller to interface with USB3300 via ULPI interface. The USB interface support only USB Host mode. The list of pin connection is shown below.

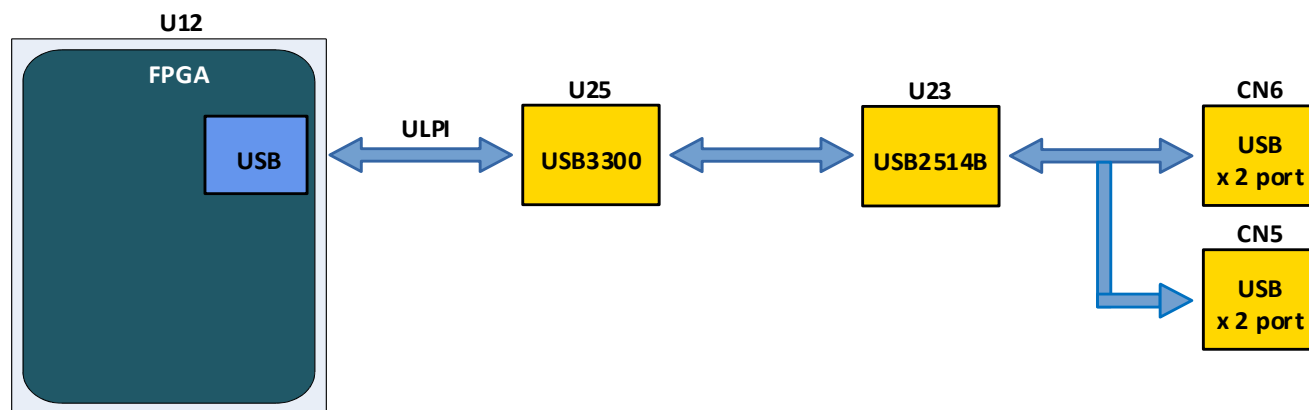


Figure 20 : EtherCAT Connection

USB signal	FPGA pin
HPS_USB_CLK	N16
HPS_USB_DAT0	E16
HPS_USB_DAT1	G16
HPS_USB_DAT2	D16
HPS_USB_DAT3	D14
HPS_USB_DAT4	A15
HPS_USB_DAT5	C14
HPS_USB_DAT6	D15
HPS_USB_DAT7	M17
HPS_USB_DIR	E14
HPS_USB_NXT	A14
HPS_USB_STP	C15

Table 7 : USB pin description

LED, Switch, and Jumper

The Cyclone V includes 1 DIP switch 1 button switch and 6 LEDs on the FPGA, and 1 DIP switch and 6 LEDs on the HPS as shown in the Figure 21. The voltage level of FPGA switch is 3.3V, and the voltage level of HPS switch is 1.5V. The button switch is used to reset the system. The voltage level of all LEDs is 3.3V. The Cyclone V has to drive high logic to turn on the LEDs, and low logic to turn off the LEDs. For the DIP switches, the Cyclone V will detect low logic if switch the DIP switch to ON. The RUN and ERR LED will show status of EtherCAT and Ethernet.

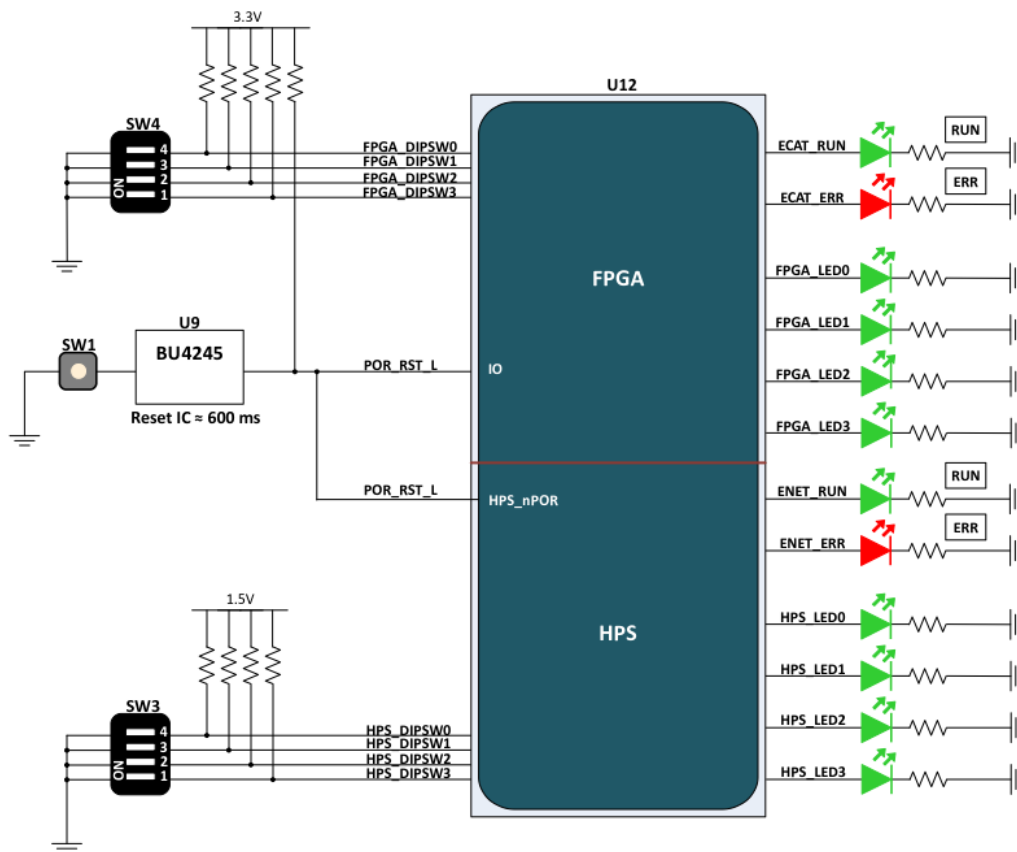


Figure 21 : LED and Switch

The 1 bit DIP switch (SW2) is used to enable and disable the JTAG chain as shown in the Figure 22. Switching to OFF is enable and switching to ON is disable.

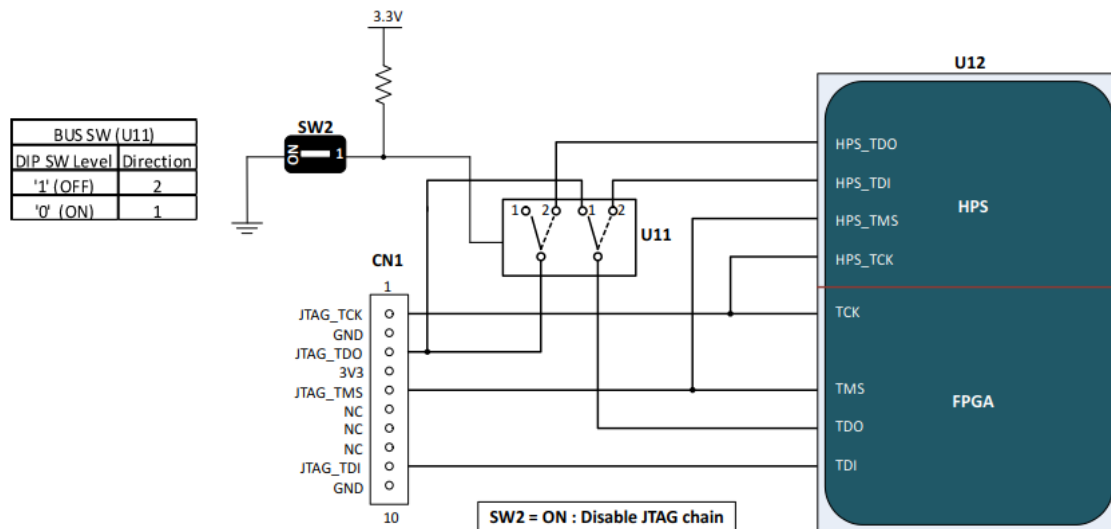
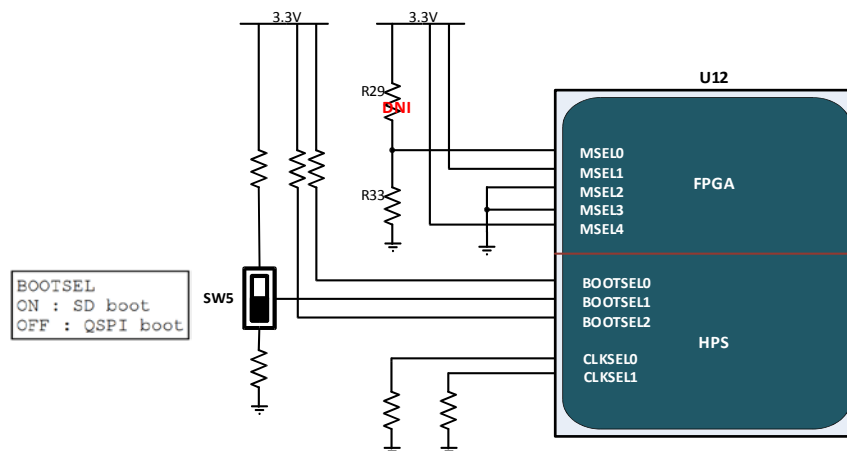


Figure 22 : JTAG Chain Switch Control

The slide switch (SW5) on the ZEKE-G board is used to select the boot mode. Two boot sources are MicroSD Card and QSPI flash as shown in the Figure 23.



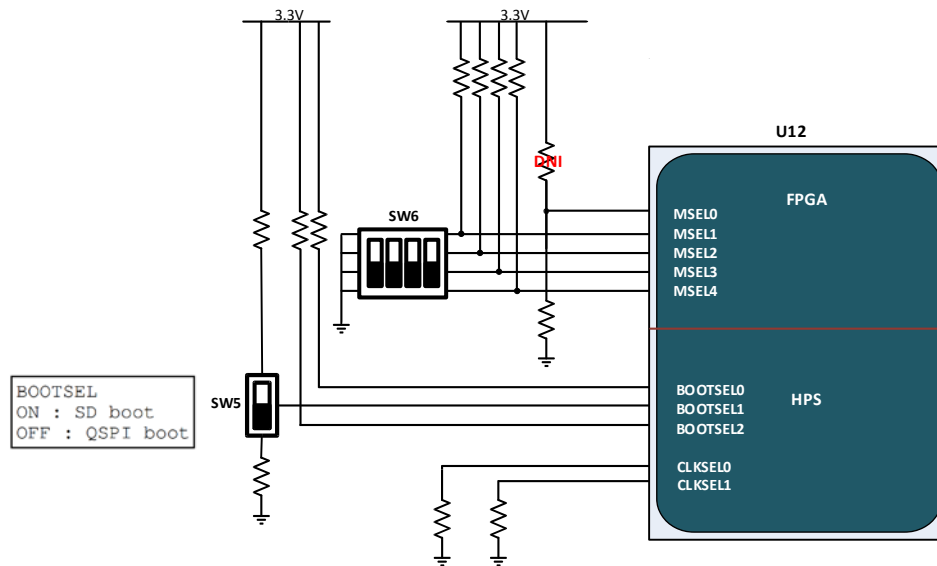


Figure 23 : slide switch (SW5)

The two LEDs (LD1 and LD12) indicate the power of the ZEKE-G board to show that there is power supply 5V and 3.3V on the board or not as shown in the Figure 24.

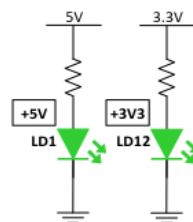


Figure 24 : Power LED

Expansion IO

The ZEKE-G board has two expansion connectors on the bottom of the board. The IO pins are directly connected between the Cyclone V and the expansion connectors. Voltage level of all pin's connection is 3.3V.

Expansion Connection Table

FPGA pin No	Signal Name	CN4 pin No	CN4 pin No	Signal Name	FPGA pin No
-	Plus5V	A1	B1	Plus5V	-
-	Plus5V	A2	B2	Plus5V	-
AA10	Plus3V3	A3	B3	Plus3V3	AA10
AA10	Plus3V3	A4	B4	Plus3V3	AA10
AG27	FPGA_GPIO[0]	A5	B5	FPGA_GPIO[1]	AF26
AG26	FPGA_GPIO[2]	A6	B6	FPGA_GPIO[3]	AG25
AH25	FPGA_GPIO[4]	A7	B7	FPGA_GPIO[5]	AH24
AF23	FPGA_GPIO[6]	A8	B8	FPGA_GPIO[7]	AG23
AH23	FPGA_GPIO[8]	A9	B9	FPGA_GPIO[9]	AC23
-	Ground	A10	B10	Ground	-
AH22	FPGA_GPIO[10]	A11	B11	FPGA_GPIO[11]	AE22
AA20	FPGA_GPIO[12]	A12	B12	FPGA_GPIO[13]	AC20
W19	FPGA_GPIO[14]	A13	B13	FPGA_GPIO[15]	AA19
Y18	FPGA_GPIO[16]	A14	B14	FPGA_GPIO[17]	AA18
V18	FPGA_GPIO[18]	A15	B15	FPGA_GPIO[19]	Y17
W17	FPGA_GPIO[20]	A16	B16	FPGA_GPIO[21]	AA16
W16	FPGA_GPIO[22]	A17	B17	FPGA_GPIO[23]	V16
AH15	FPGA_GPIO[24]	A18	B18	FPGA_GPIO[25]	AG15
AH14	FPGA_GPIO[26]	A19	B19	FPGA_GPIO[27]	AC18
-	Ground	A20	B20	Ground	-
AJ10	FPGA_GPIO[28]	A21	B21	FPGA_GPIO[29]	AK9
AJ9	FPGA_GPIO[30]	A22	B22	FPGA_GPIO[31]	AK8
AK7	FPGA_GPIO[32]	A23	B23	FPGA_GPIO[33]	AJ7
AK6	FPGA_GPIO[34]	A24	B24	FPGA_GPIO[35]	AJ6
AJ5	FPGA_GPIO[36]	A25	B25	FPGA_GPIO[37]	AK4
AJ4	FPGA_GPIO[38]	A26	B26	FPGA_GPIO[39]	AK3
AK2	FPGA_GPIO[40]	A27	B27	FPGA_GPIO[41]	AJ2
AJ1	FPGA_GPIO[42]	A28	B28	FPGA_GPIO[43]	AH2
AG2	FPGA_GPIO[44]	A29	B29	FPGA_GPIO[45]	AG1
-	Ground	A30	B30	Ground	-
AH9	FPGA_GPIO[46]	A31	B31	FPGA_GPIO[47]	AF9

FPGA pin No	Signal Name	CN4 pin No	CN4 pin No	Signal Name	FPGA pin No
AH8	FPGA_GPIO[48]	A32	B32	FPGA_GPIO[49]	AH7
AG8	FPGA_GPIO[50]	A33	B33	FPGA_GPIO[51]	AG7
AF8	FPGA_GPIO[52]	A34	B34	FPGA_GPIO[53]	AG6
AH5	FPGA_GPIO[54]	A35	B35	FPGA_GPIO[55]	AH4
AH3	FPGA_GPIO[56]	A36	B36	FPGA_GPIO[57]	AG5
AG3	FPGA_GPIO[58]	A37	B37	FPGA_GPIO[59]	AF6
AF5	FPGA_GPIO[60]	A38	B38	FPGA_GPIO[61]	AF4
AD9	FPGA_GPIO[62]	A39	B39	FPGA_GPIO[63]	AE11
-	Ground	A40	B40	Ground	-
AC9	FPGA_GPIO[64]	A41	B41	FPGA_GPIO[65]	AD11
AB17	FPGA_GPIO[66]	A42	B42	FPGA_GPIO[67]	AD17
AG17	FPGA_GPIO[68]	A43	B43	FPGA_GPIO[69]	Y19
Y16	FPGA_GPIO[70]	A44	B44	FPGA_GPIO[71]	AE14
AE13	FPGA_GPIO[72]	A45	B45	FPGA_GPIO[73]	AH13
AG13	FPGA_GPIO[74]	A46	B46	FPGA_GPIO[75]	AF13
AH12	FPGA_GPIO[76]	A47	B47	FPGA_GPIO[77]	AG12
AE12	FPGA_GPIO[78]	A48	B48	FPGA_GPIO[79]	AG11
AF11	FPGA_GPIO[80]	A49	B49	FPGA_GPIO[81]	AH10
AG10	FPGA_GPIO[82]	A50	B50	FPGA_GPIO[83]	AF10

Table 8 : CN4 pin description

FPGA pin No	Signal Name	CN49pin No	CN9 pin No	Signal Name	FPGA pin No
-	Plus5V	A1	B1	Plus5V	-
-	Plus5V	A2	B2	Plus5V	-
AA10	Plus3V3	A3	B3	Plus3V3	AA10
AA10	Plus3V3	A4	B4	Plus3V3	AA10
AE19	FPGA_GPIO[84]	A5	B5	FPGA_GPIO[85]	AD19
AD20	FPGA_GPIO[86]	A6	B6	FPGA_GPIO[87]	V17
AD21	FPGA_GPIO[88]	A7	B7	FPGA_GPIO[89]	AG22
AB21	FPGA_GPIO[90]	A8	B8	FPGA_GPIO[91]	AE24
AJ11	FPGA_GPIO[92]	A9	B9	FPGA_GPIO[93]	AK11
-	Ground	A10	B10	Ground	-
AJ12	FPGA_GPIO[94]	A11	B11	FPGA_GPIO[95]	AK12
AK13	FPGA_GPIO[96]	A12	B12	FPGA_GPIO[97]	AJ14
AK14	FPGA_GPIO[98]	A13	B13	FPGA_GPIO[99]	AK16
AJ16	FPGA_GPIO[100]	A14	B14	FPGA_GPIO[101]	AJ17
AK23	FPGA_GPIO[102]	A15	B15	FPGA_GPIO[103]	AK24
AJ24	FPGA_GPIO[104]	A16	B16	FPGA_GPIO[105]	AJ25
AF16	FPGA_GPIO[106]	A17	B17	FPGA_GPIO[107]	AG16
AH17	FPGA_GPIO[108]	A18	B18	FPGA_GPIO[109]	AE17
AG18	FPGA_GPIO[110]	A19	B19	FPGA_GPIO[111]	AH18
-	Ground	A20	B20	Ground	-
AF18	FPGA_GPIO[112]	A21	B21	FPGA_GPIO[113]	AF19
AK26	FPGA_GPIO[114]	A22	B22	FPGA_GPIO[115]	AJ26
AJ27	FPGA_GPIO[116]	A23	B23	FPGA_GPIO[117]	AK27
AH27	FPGA_GPIO[118]	A24	B24	FPGA_GPIO[119]	AH28
AK28	FPGA_GPIO[120]	A25	B25	FPGA_GPIO[121]	AK29
AH29	FPGA_GPIO[122]	A26	B26	FPGA_GPIO[123]	AH30
AG30	FPGA_GPIO[124]	A27	B27	FPGA_GPIO[125]	AF30
AH19	FPGA_GPIO[126]	A28	B28	FPGA_GPIO[127]	AH20
AF20	FPGA_GPIO[128]	A29	B29	FPGA_GPIO[129]	AG20
-	Ground	A30	B30	Ground	-
AK18	FPGA_GPIO[130]	A31	B31	FPGA_GPIO[131]	AK19
AJ19	FPGA_GPIO[132]	A32	B32	FPGA_GPIO[133]	AJ20
AK21	FPGA_GPIO[134]	A33	B33	FPGA_GPIO[135]	AJ21
AK22	FPGA_GPIO[136]	A34	B34	FPGA_GPIO[137]	AJ22
AG21	FPGA_GPIO[138]	A35	B35	FPGA_GPIO[139]	AE18
AF21	FPGA_GPIO[140]	A36	B36	FPGA_GPIO[141]	AE23
AF24	FPGA_GPIO[142]	A37	B37	FPGA_GPIO[143]	AD24
AF25	FPGA_GPIO[144]	A38	B38	FPGA_GPIO[145]	AA21

FPGA pin No	Signal Name	CN49pin No	CN9 pin No	Signal Name	FPGA pin No
AC22	FPGA_GPIO[146]	A39	B39	FPGA_GPIO[147]	AB22
-	Ground	A40	B40	Ground	-
AE27	FPGA_GPIO[148]	A41	B41	FPGA_GPIO[149]	AB23
AB25	FPGA_GPIO[150]	A42	B42	FPGA_GPIO[151]	AG28
AE28	FPGA_GPIO[152]	A43	B43	FPGA_GPIO[153]	AF28
AF29	FPGA_GPIO[154]	A44	B44	FPGA_GPIO[155]	AB26
AA24	FPGA_GPIO[156]	A45	B45	FPGA_GPIO[157]	AA25
B26	HPS_GPIO[0]	A46	B46	HPS_GPIO[1]	B25
A25	HPS_GPIO[2]	A47	B47	HPS_GPIO[3]	C25
H20	HPS_GPIO[4]	A48	B48	HPS_GPIO[5]	B23
G22	HPS_GPIO[6]	A49	B49	HPS_GPIO[7]	B22
C23	HPS_UART_RX	A50	B50	HPS_UART_TX	D22

Table 9 : CN9 pin description

Start Using ZEKE-G

Power Up ZEKE-G Board

Firstly, plug the power supply in to CN10, and see the power LEDs on the ZEKE-G board. LD1 for 5V and LD12 for 3.3V should be bright. The Figure 25 shows the location of power connector, power on LED, and power test points.

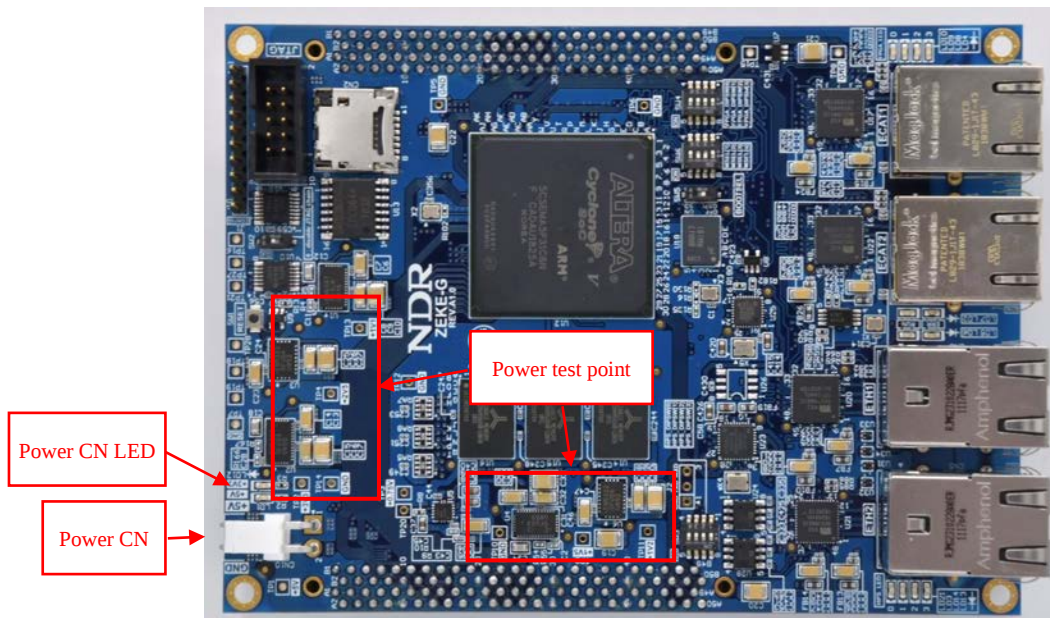


Figure 25 : Location of ZEKE-G Power

Step of Creating HPS on QSYS

1. Open Quartus Prime. Click at Tools -> QSYS as shown in the Figure 26.

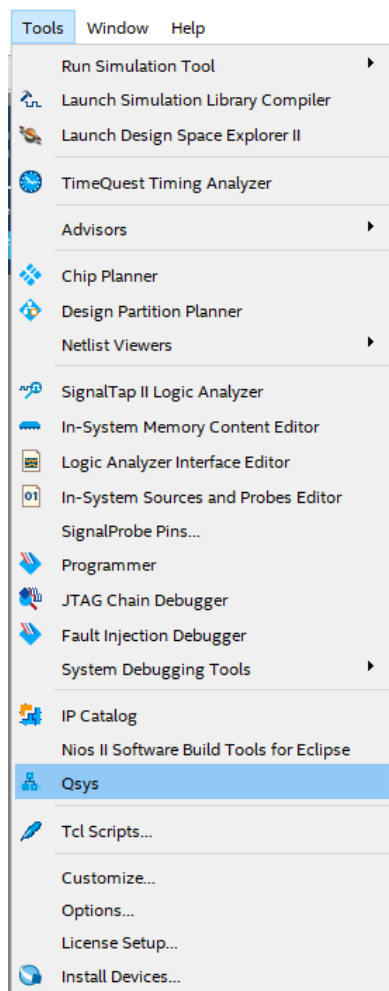


Figure 26 : QSYS Menu

2. On IP Catalog tab, search the word “hps”, then Arria V/Cyclone V Hard Processor System will appear as shown in the Figure 27. Double click it.

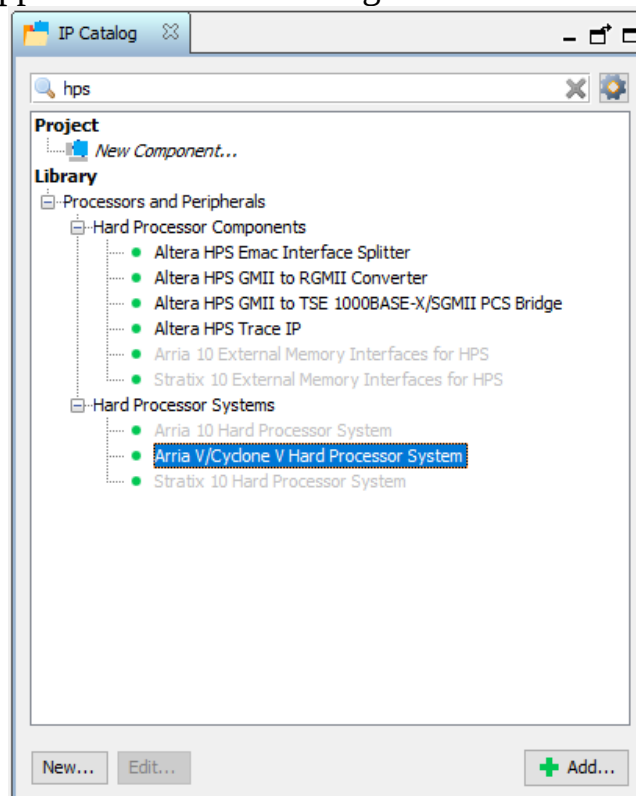


Figure 27 : HPS on IP Catalog

3. The default tab is FPGA Interfaces as shown in the Figure 28. Click the box according to the design.

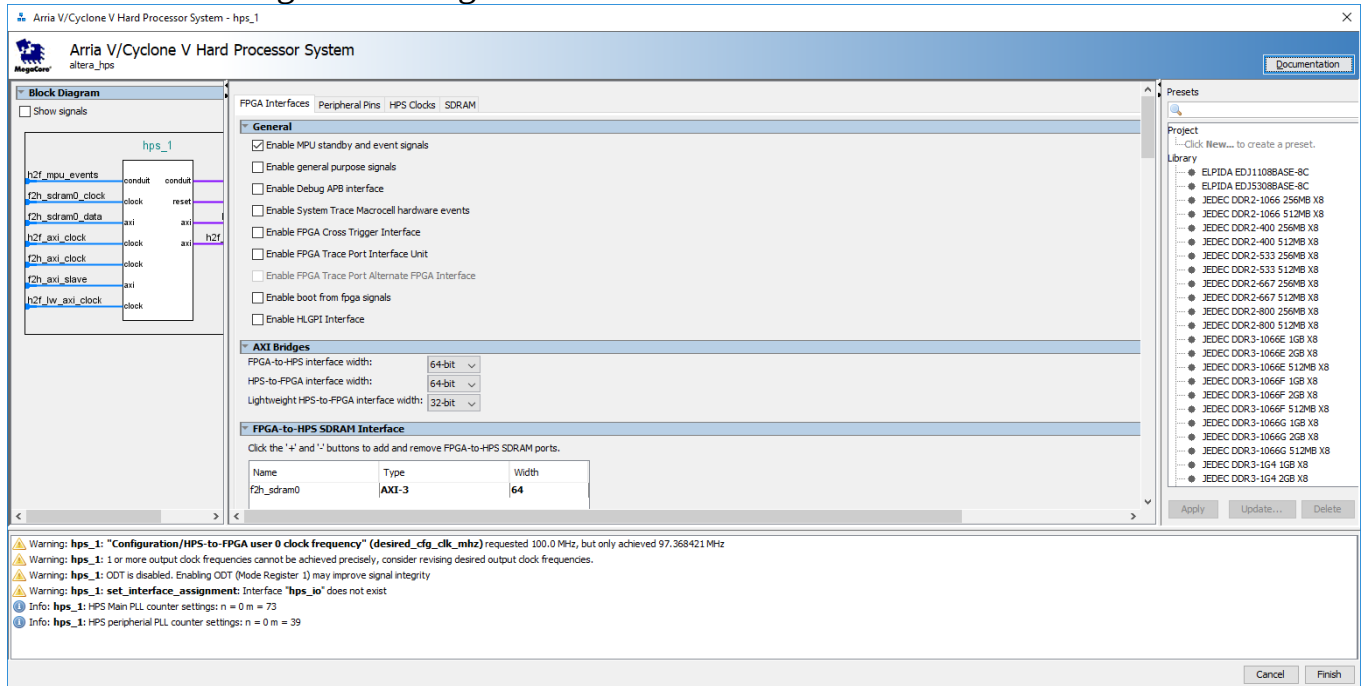


Figure 28 : Arria V/Cyclone V Hard Processor System

4. On Peripheral Pins tab, set the function pin and mode that is used in the design as shown in the Figure 29.

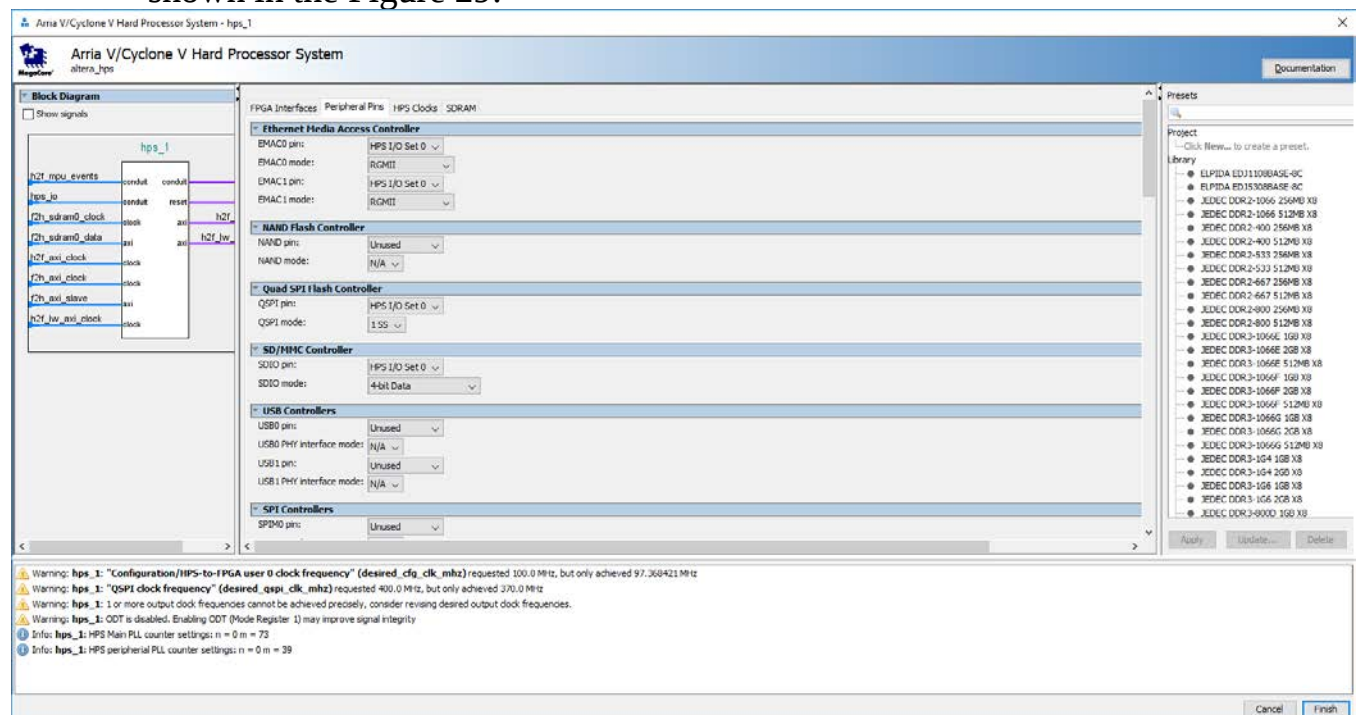


Figure 29 : Peripheral Pins of HPS

- On SDRAM tab, select DDR3 in the box of SDRAM protocol, and the other parameters as shown in the Figure 30. Then, click finish.

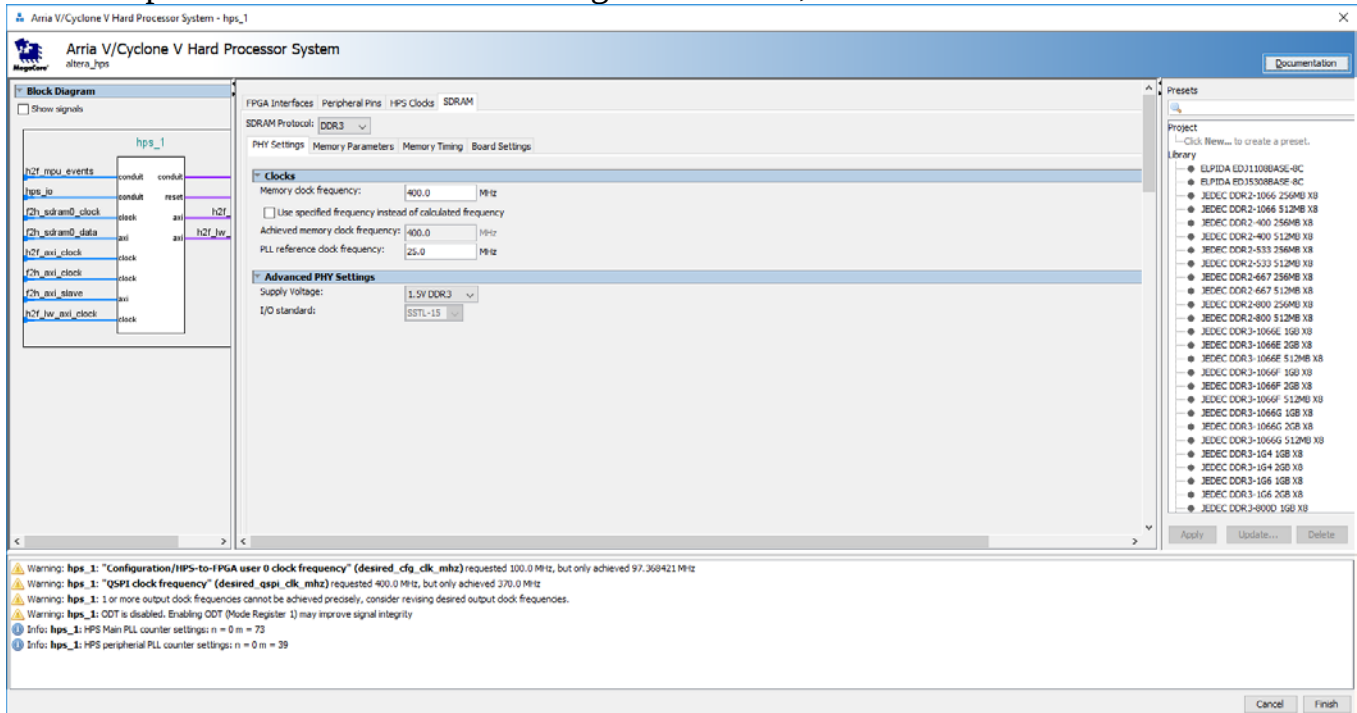


Figure 30 : SDRAM of HPS

6. Do the connection and address mapping of the design. Save the file if you have finished.

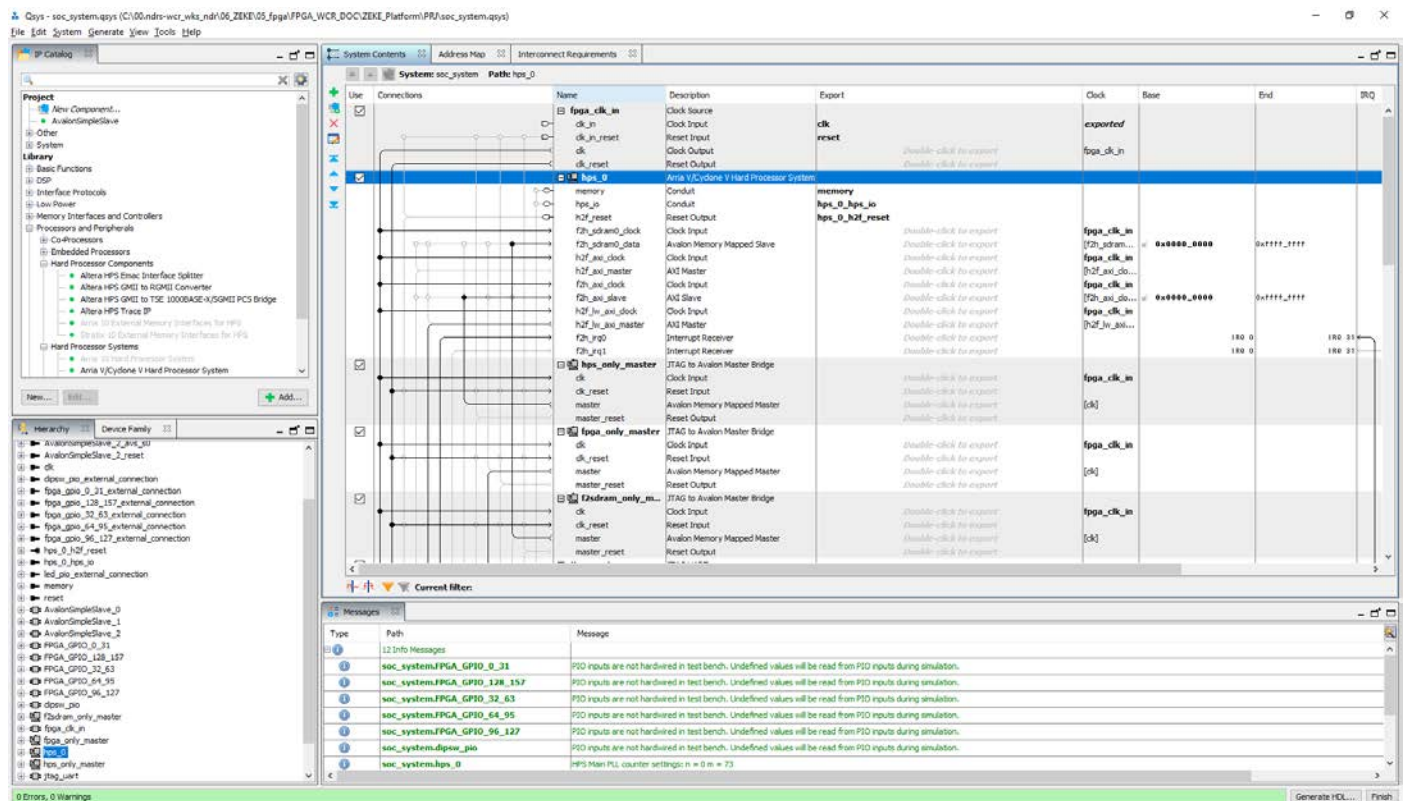


Figure 31 : HPS Design on QSYS

7. Click **Generate HDL**. The windows in the Figure 32 will appear. Select the format

file in Verilog or VHDL, and then click Generate.

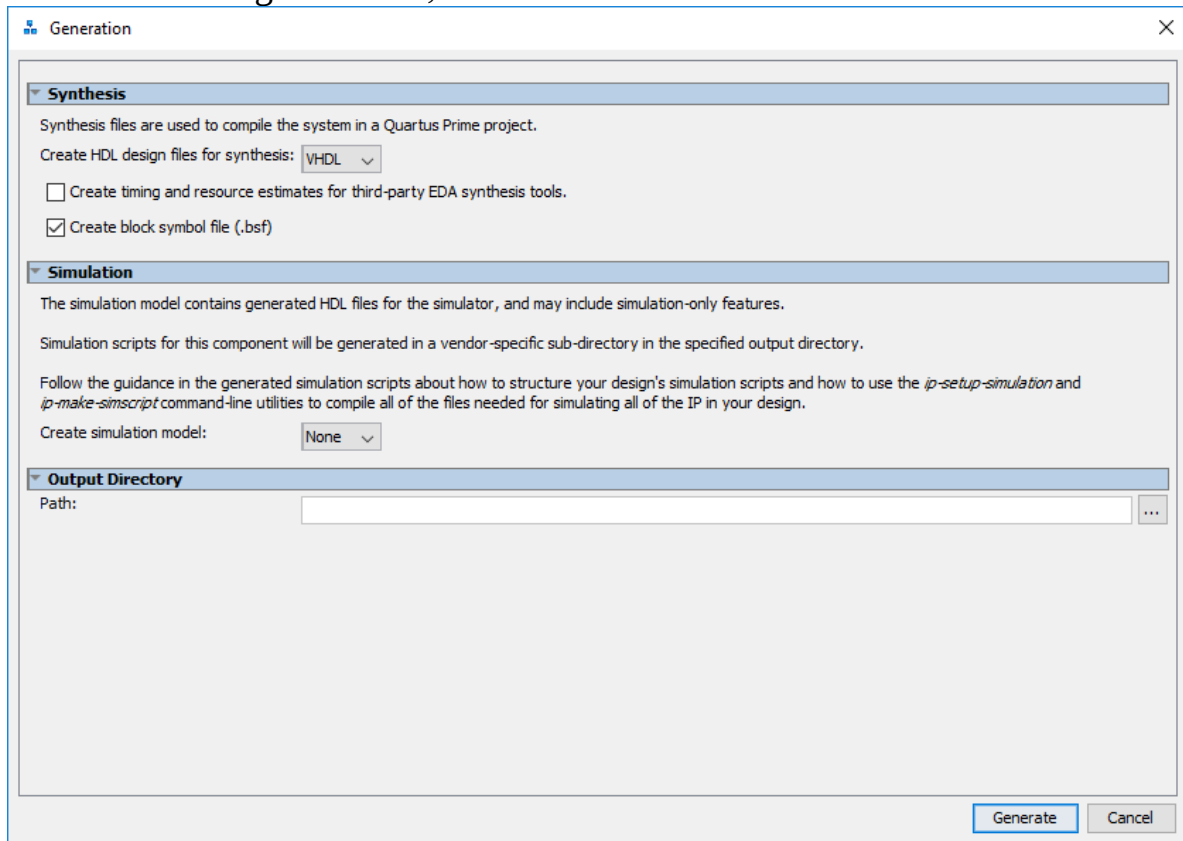


Figure 32 : QSYS Generate File

Step of Gernerating SOF File

1. After you have finished creating HPS on QSYS, and TOP File of your design. Open Quartus Prime. Go to Assignment -> Settings as shown in the Figure 33.

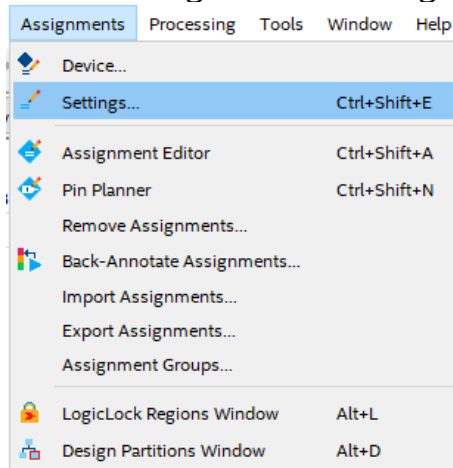


Figure 33 : Settings Menu in Quartus Prime

2. In Category, click Files, and add files to your project (QSYS file and/or TOP File). Then, click OK.

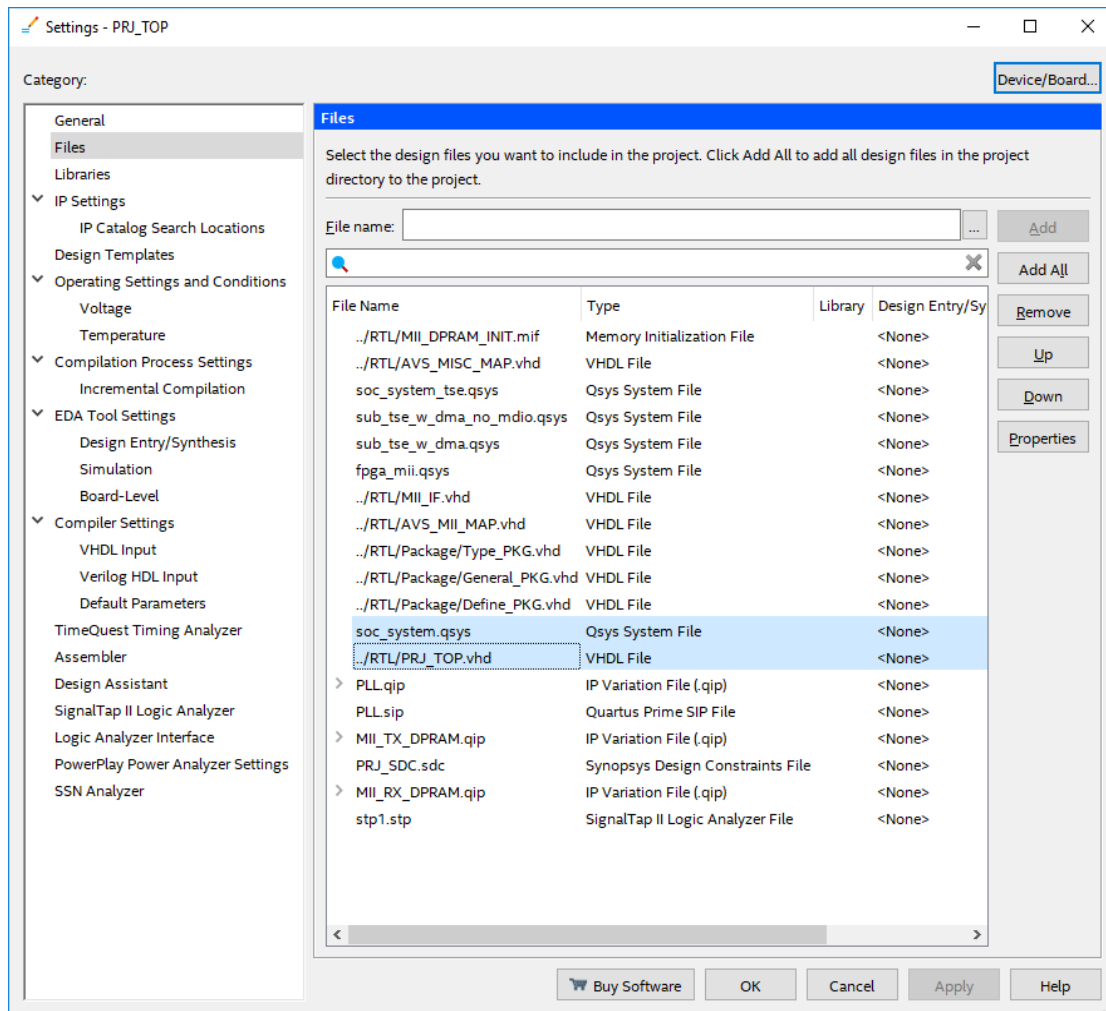


Figure 34 : Add File to Project

3. Click Processing -> Start Compilation to compile the project.

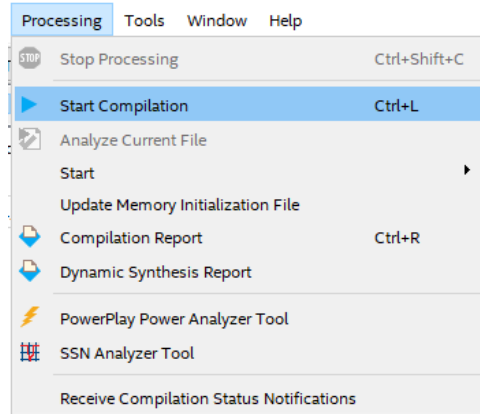


Figure 35 : Start Complication

4. After finished compiling the project, you will get SOF file in your output_files folder.

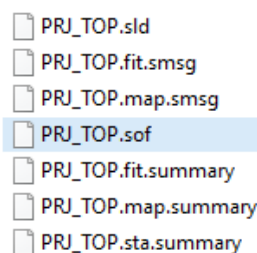


Figure 36 : SOF Output File

Step of Creating JIC File

1. Open Quartus Prime. Go to File -> Convert Programming Files as shown in the Figure 37.

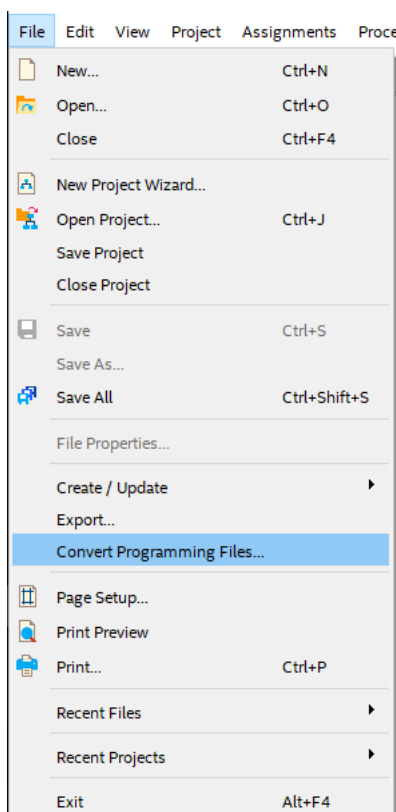


Figure 37 : Convet Programming Files Menu

2. Change Programming file type to JIC file as shown in the Figure 38.

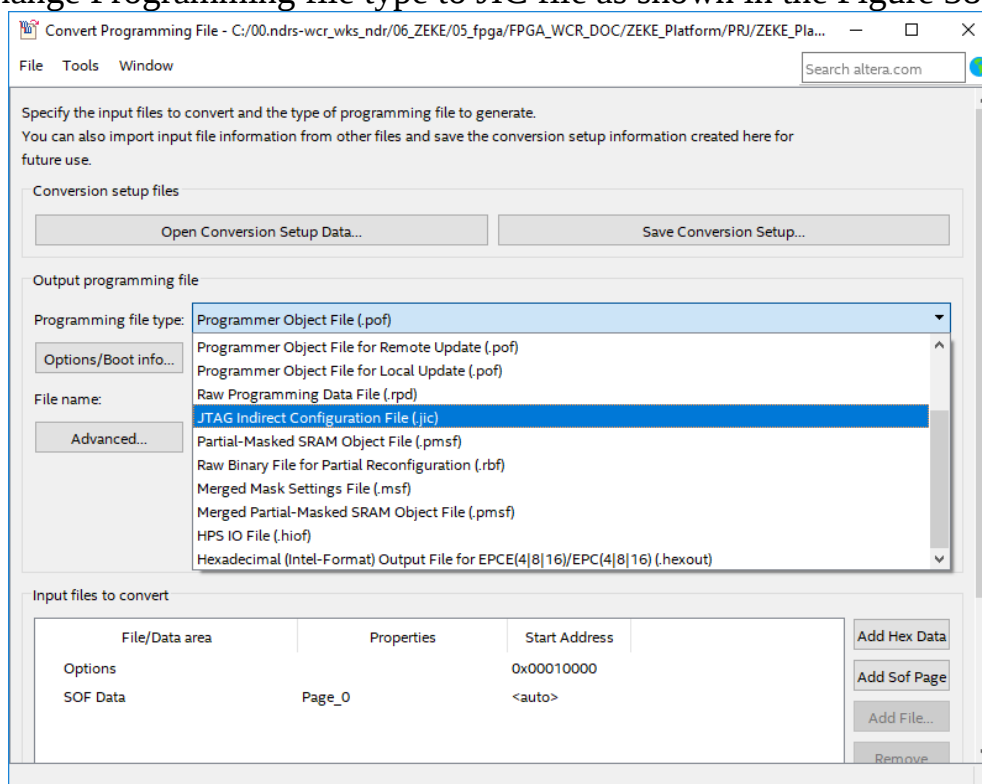


Figure 38 : Programming File Type

3. Select Configuration device. Select EPCQ64A for the ZEKE-G board, and then add Flash Loader and SOF Data by following the list below. Click Generate to get JIC file.

- Configuration device : EPCQ64A
- Flash Loader : 5CSEMA5F31
- SOF Data : SOF file from compilation

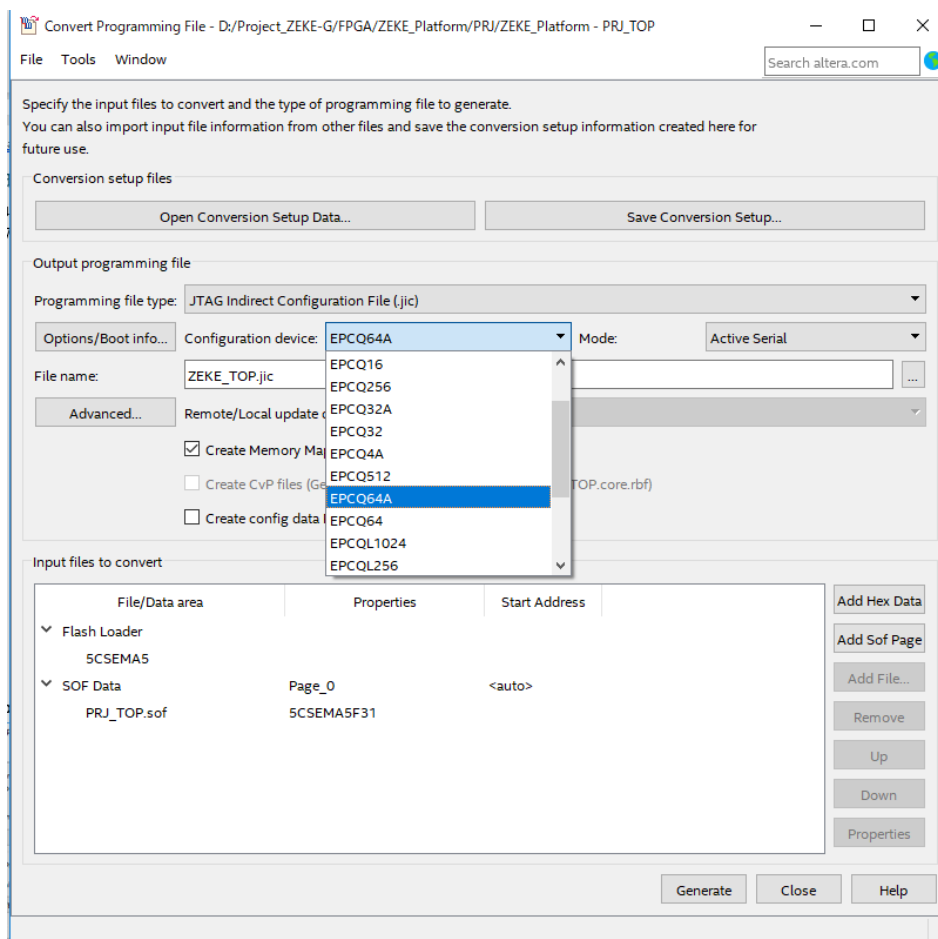


Figure 39 : Setting SOF File and Flash Loader

4. The JIC file is created in output_files folder.

PRJ_TOP.cdf
 PRJ_TOP.done
 PRJ_TOP.jdi
ZEKE_TOP.jic

Figure 40 : JIC Output File

Step of Programming by JTAG

1. Open Quartus Prime. Click Tools -> Programmer to open programmer software.

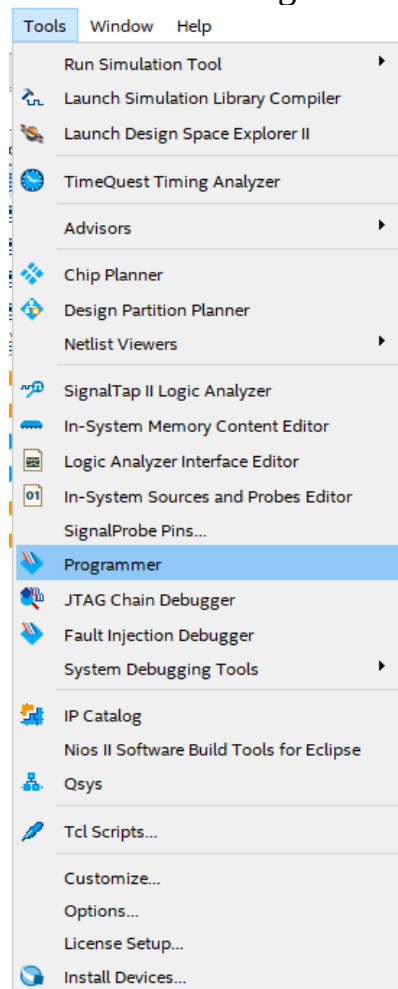


Figure 41 : Programmer Menu

2. Select Hardware Setup of progammer device.

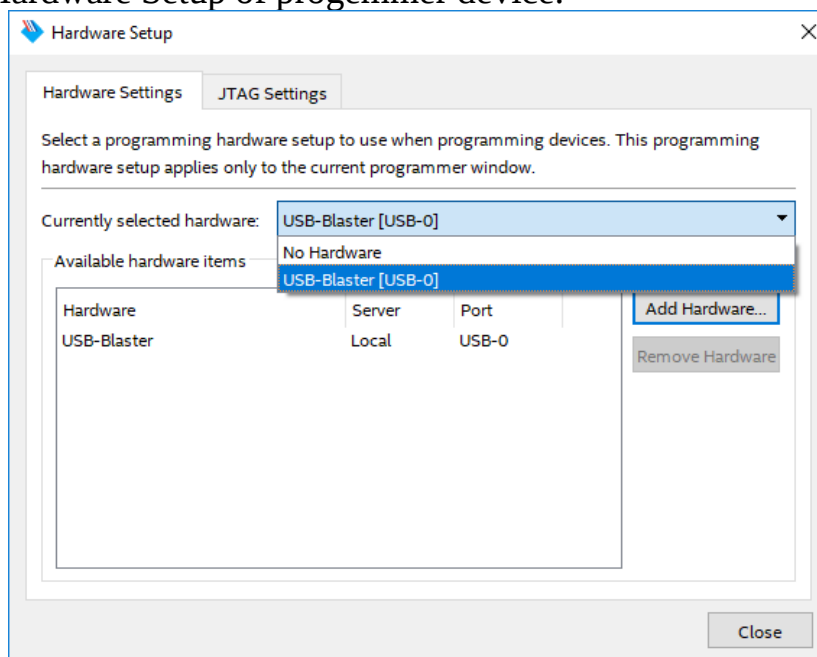


Figure 42 : Progeammer Device Setup

3. Add JIC file to the programmer. Check the box in Program/Configure column as

shown in the Figure 43. Make sure that SW2 is OFF (enable the JTAG chain), and then start to program.

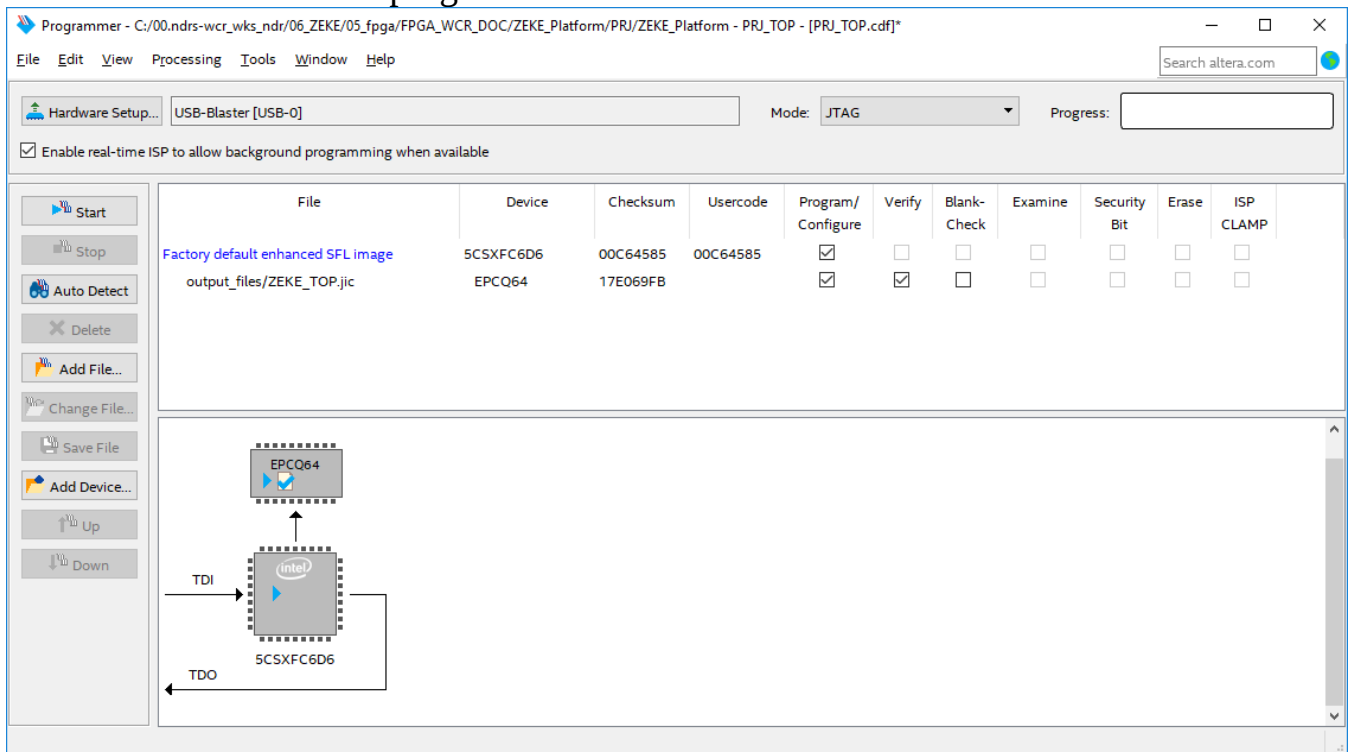


Figure 43 : Program the ZEKE-G board

Associated Product

OSCAR Board

The OSCAR board is an evaluation board which contains MAX 10, two of 10/100 Ethernet (PHY), SDRAM, EEPROM, NOR flash memory LED, rotary switch, and expansion connector. For more information please see on OSCAR Board User Manual. The look of the OSCAR board is shown in the Figure 44.

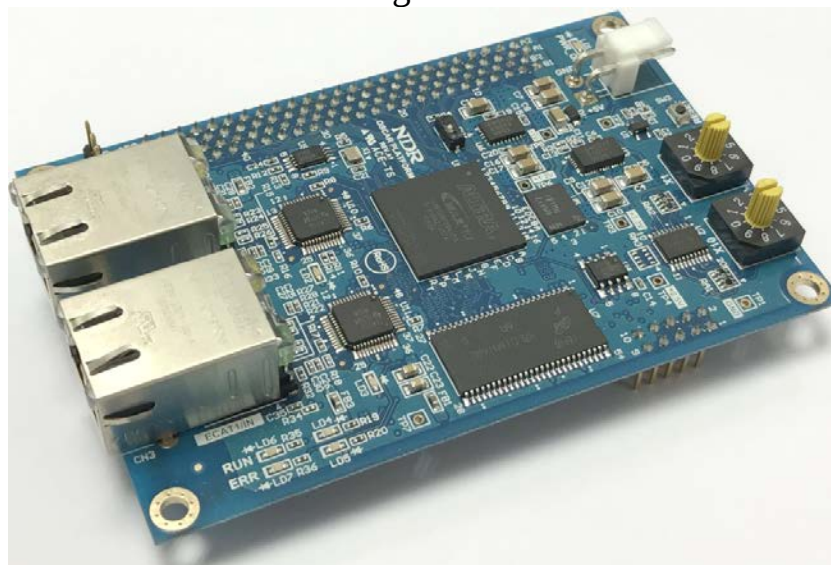


Figure 44 : OSCAR Board

ZEKE Board

ZEKE board is an evaluation board which contains Cyclone V System-on-Chip (SoC), DDR3 memory, two of 10/100/1000 Ethernet (PHY), two of 10/100 Ethernet (PHY), MicroSD Card connector, NOR flash memory along with user IO such as DIP switch, LED, and expansion connector. For more information please see on ZEKE Board User Manual. The look of the ZEKE board is shown in the Figure 45.



Figure 45 : ZEKE Board

Additional Information

Getting Help

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Revision History

Date	Revision	Changes list
2019-11-11	0.1	First draft