

OSCAR Board User Manual

Revision 0.1

October 5, 2017

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Overview

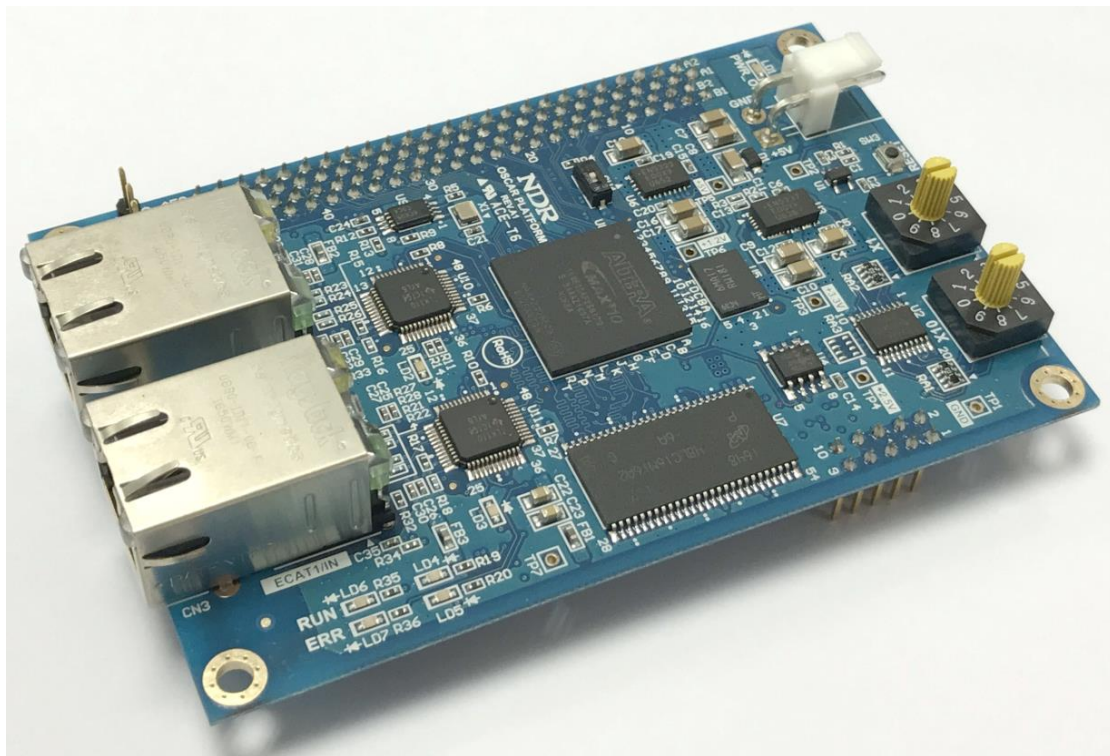


Figure 1 : The OSCAR Board

The OSCAR board is an evaluation board which contains MAX 10, two of 10/100 Ethernet (PHY), SDRAM, EEPROM, NOR flash memory LED, rotary switch, and expansion connector. The OSCAR board enables EtherCAT implementation, and this allows to use category 5 cable or above. User IO and expansion connector can be used to control the other device or board depending on user application.

Package Contents

- OSCAR Board
- OSCAR Board User Manual
- 5V DC Power Supply

Board Overview

The components on the OSCAR board are shown in the Figure below.

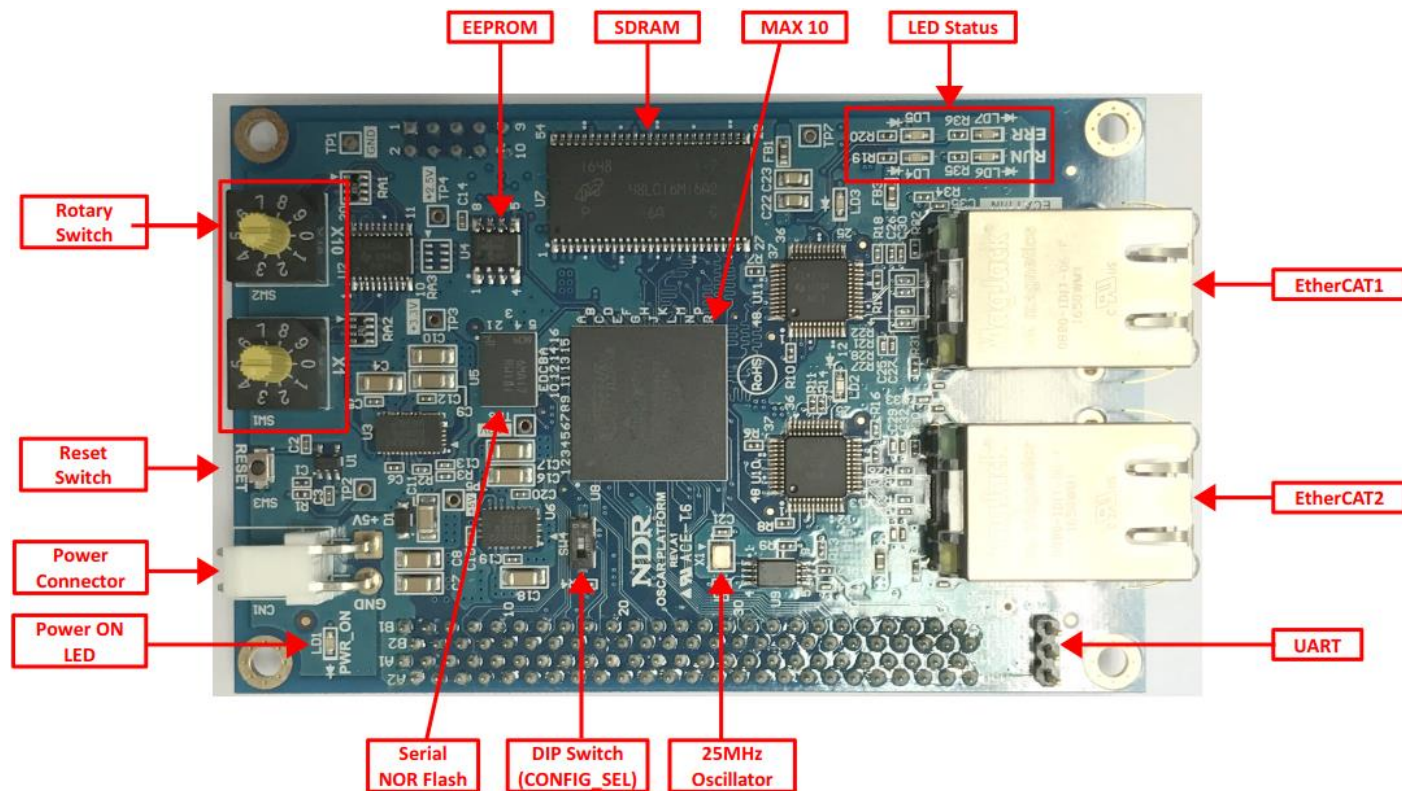


Figure 2 : Top View of OSCAR Board

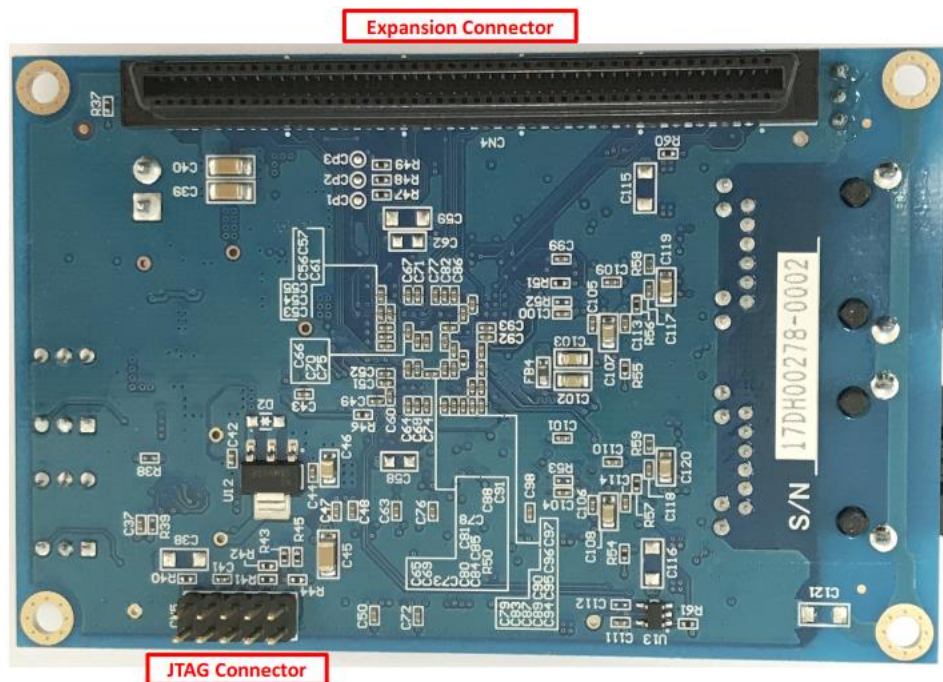


Figure 3 : Bottom View of OSCAR Board

Design Specification

- Power Connector : B2PS-VH(LF)(SN)
- FPGA : 10M50DAF256C7G (MAX 10)
- SDRAM x2 : MT48LC16M16A2P-6A:G (256Mb)
- EEPROM : 24LC256-I/SN (32Kb)
- Serial NOR Flash : MT25QL512ABB8E12-0SIT (512Mb)
- EtherCAT x2 : TLK110PTR
- UART : 3 Pins (RX, TX, GND)
- LED : IO LED x2, Status LED x4, Power LED x1
- Button Switch : System Reset Switch
- DIP Switch : 1 bit for CONFIG_SEL signal
- Rotary Switch x2 : Rotary Switch 4 bits for decimal number 2 digit (00-99)
- Expansion IO : FX2C-100S-1.27DSA (ADDR + DATA + IO + UART + Power)

Block Diagram

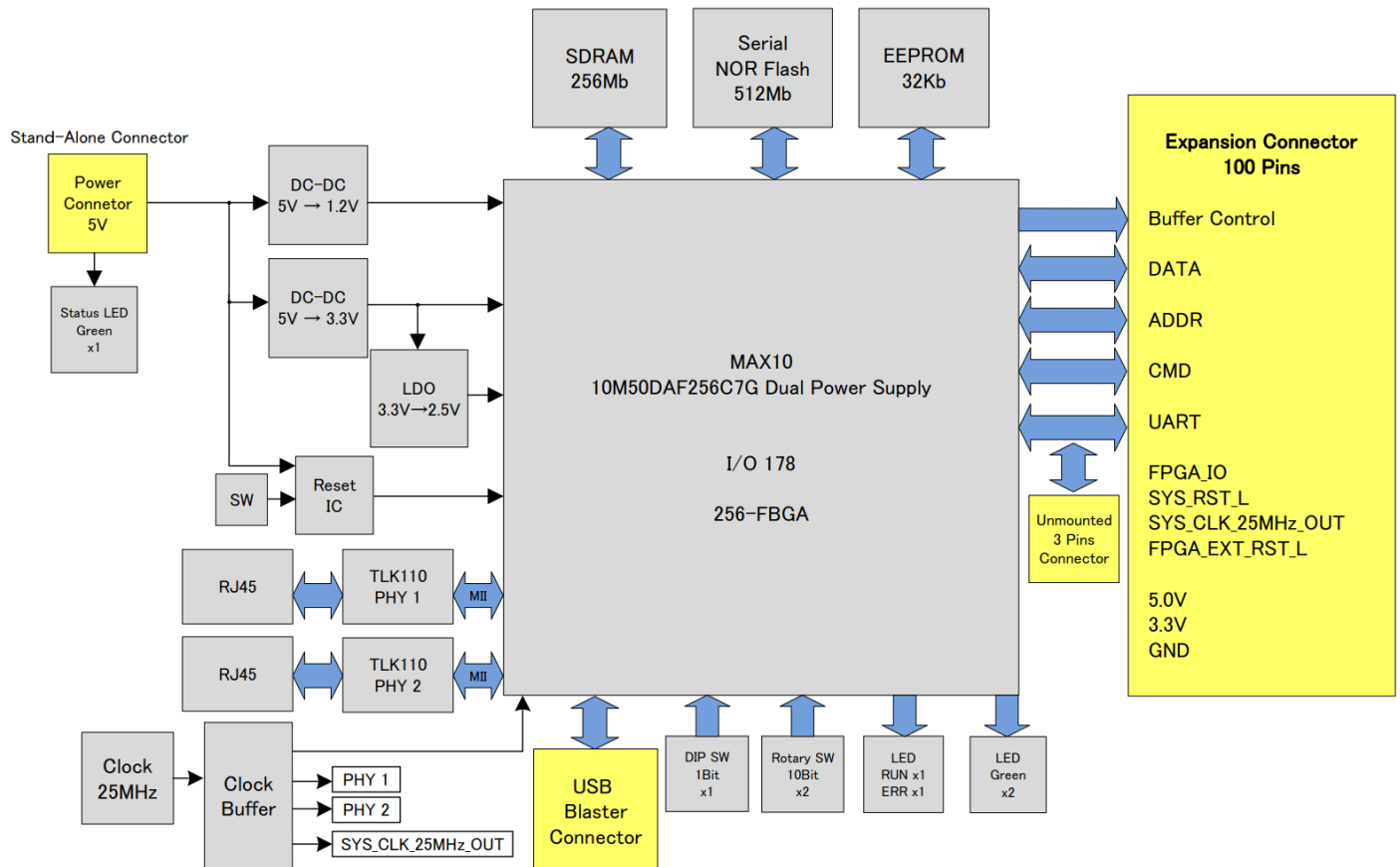


Figure 4 : Block Diagram

Power Supply

The OSCAR board uses 5V power supply that the output current of power supply recommends at least 1A. The connector of the power input is a 2-position right angle header connector (CN1), and the part number is B2PS-VH(LF)(SN). After plug the power supply in, the power on LED (LD1), that is beside power connector, should be bright. The LD1 is green color, and named PWR_ON. In the other way to supply 5V to the OSCAR board, connect the board that generates 5V to the expansion connector (CN4).

Power Management

After generating 5V power supply to the OSCAR board, DCDC converter 5V to 1.2V and DCDC converter 5V to 3.3V will work. LDO uses power 3.3V, and generate 2.5V to MAX 10. The power diagram is shown in the Figure 5.

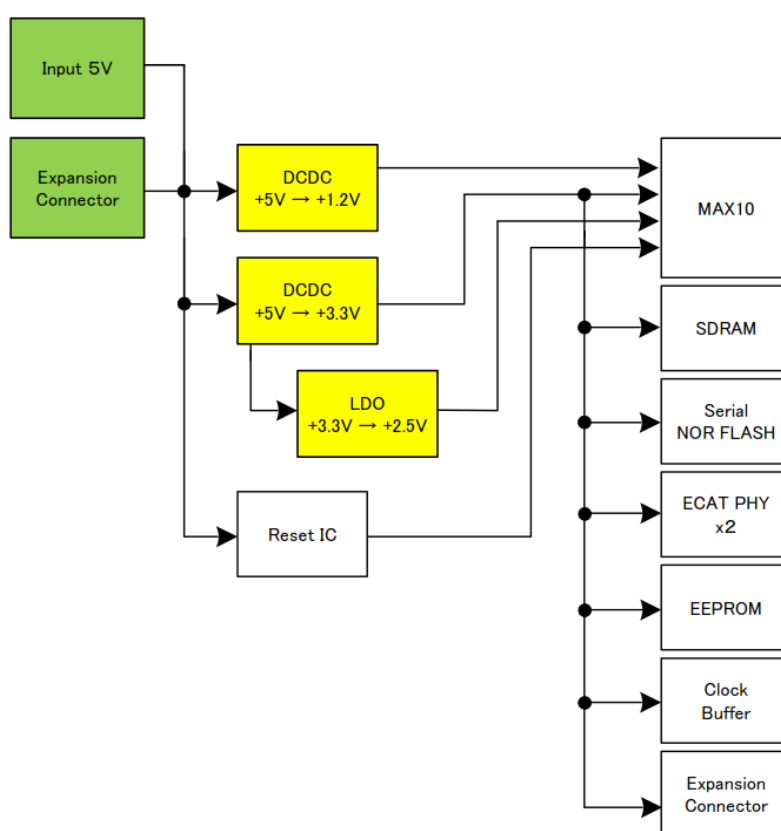


Figure 5 : Power Block Diagram

The OSCAR board use MAX 10 (10M50DAF256C7G) device to control the board. The MAX 10 is designed for dual configuration.

FPGA Power

This MAX 10 uses dual supply mode so it requires voltage level 1.2V and 2.5V. The voltage level of all IO banks is 3.3V. Therefore, the MAX 10 supports only 3.3V interface.

FPGA Configuration

The MAX 10 can use two image files to configure (dual configuration). Configuration select (CONFIG_SEL) that controlled by SW4 is uses to choose the image files for configuration. If CONFIG_SEL is '0' (SW4 is ON), configure from image 0. If CONFIG_SEL is '1' (SW4 is OFF), configure from image 1. The OSCAR board configuration is shown in the Figure 6.

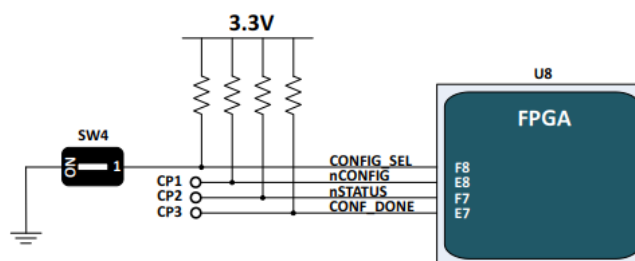


Figure 6 : FPGA Configuration

JTAG

To program MAX 10 device, you can program via JTAG connector (CN5) at the bottom of the board. The JTAG connection is shown in the Figure 7. JTAG_EN can be controlled by the expansion board.

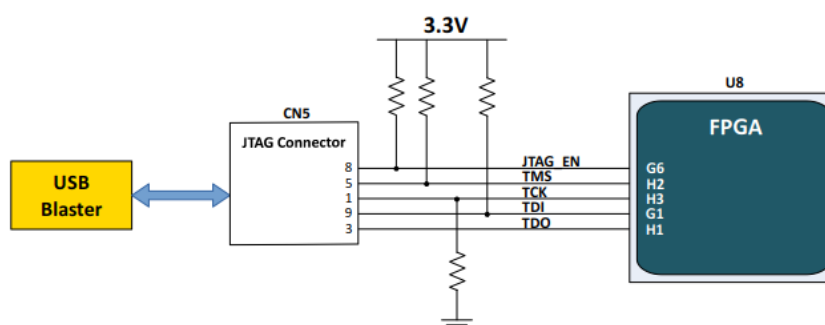


Figure 7 : JTAG Connection

Clock Source

The clock oscillator (SG-210STF25.000000MHzL) on the OSCAR board is 25 MHz 50 ppm. The OSCAR board has only one clock source connected to clock buffer, and generate to MAX 10, two EtherCAT PHY chips, and expansion connector. The Figure 8 shows the diagram of clock source on the OSCAR board.

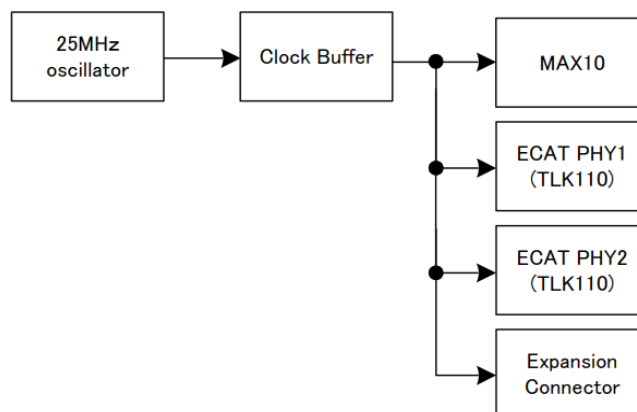


Figure 8 : Clock Source

Reset System

The OSCAR board has two choices to reset the system, that are, resetting by ON/OFF power supply and pushing button switch (SW1). The reset time is about 600 ms that is made by reset IC (BU4245G-TR) with detection voltage 4.5V. The reset system is shown in the Figure 9.

If you want to reset EtherCAT PHY chips, you can reset by FPGA IO pin P6 to low level. Then, all EtherCAT PHY chips will be reseted.

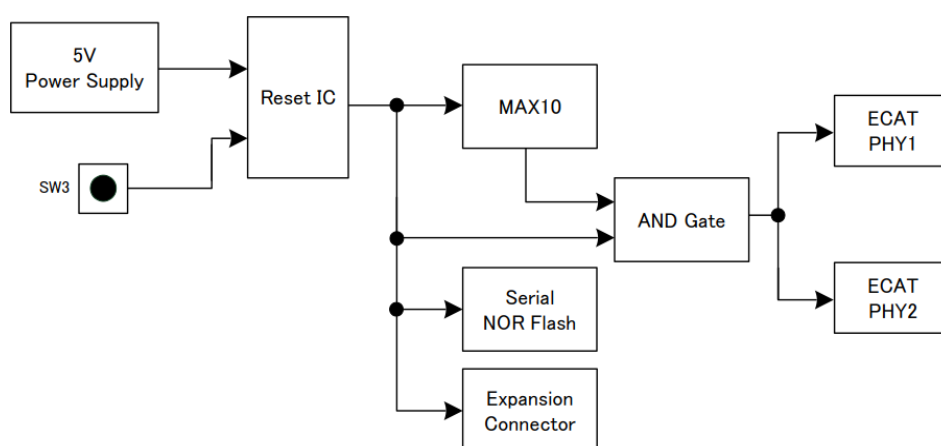


Figure 9 : Reset System

SDRAM

The memory size of SDRAM (MT48LC16M16A2P-6A:G) is 256Mb x 16, and it is designed to be a volatile memory of the OSCAR board. The SDRAM uses voltage level 3.3V as shown in the Figure 10.

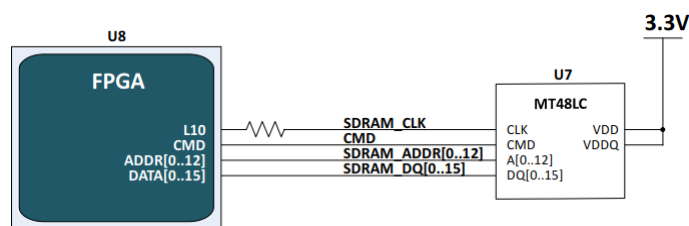


Figure 10 : SDRAM

EEPROM

The EEPROM (24LC256-I/SN) is used to be configuration memory with the size of 32Kb x 8. The EEPROM communicates to the MAX 10 by I2C protocol. This is a non-volatile memory, and used to save the programming file for configuration.

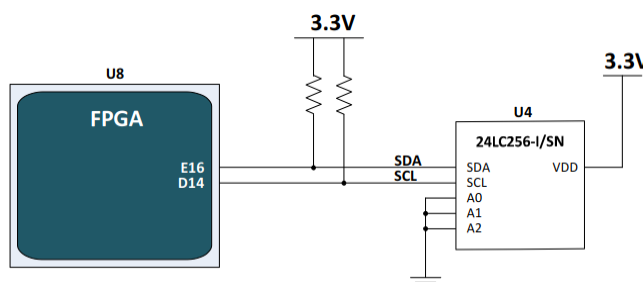


Figure 11 : EEPROM

Serial NOR Flash

The OSCAR board uses serial NOR flash (MT25QL512ABB8E12-0SIT) to save the programming file. The size of this serial NOR flash is 512 Mb. To program the serial NOR flash, you can program via JTAG connector.

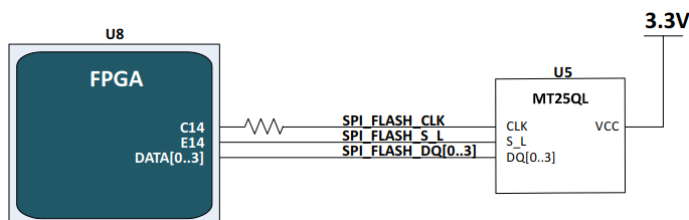


Figure 12 : Serial NOR Flash

EtherCAT

EtherCAT PHY chips (TLK110PTR) are used to design on the OSCAR board to interface with EtherCAT. The EtherCAT PHY is 10/100Mbps Ethernet physical layer transceiver. There are two EtherCAT PHY chips on the OSCAR board, and both are connected to the FPGA (3.3V). After power-up, the EtherCAT PHY starts with auto negotiation enabled, advertising 10/100 link speeds and half/full duplex. The connection and the list of pin connection are shown below.

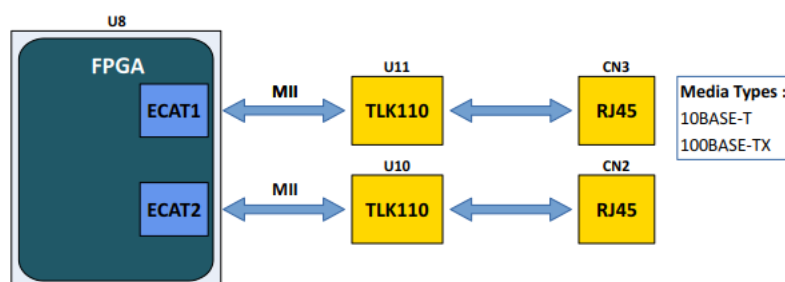


Figure 13 : EtherCAT Connection

	EtherCAT1	EtherCAT2
PHYAD[4..0]	"00001"	"00011"

Figure 14 : EtherCAT Address

FPGA Pin1	EtherCAT1	FPGA Pin2	EtherCAT2
P6	PHY1_2_RESET_L	P6	PHY1_2_RESET_L
R8	PHY1_2_MDCLK	R8	PHY1_2_MDCLK
T9	PHY1_2_MDIO	T9	PHY1_2_MDIO
M9	PHY1_RX_CLK	P8	PHY2_RX_CLK
T11	PHY1_RX_DV	R7	PHY2_RX_DV
R10	PHY1_RX_ER	T8	PHY2_RX_ER
M10	PHY1_RXD[0]	T4	PHY2_RXD[0]
T13	PHY1_RXD[1]	M7	PHY2_RXD[1]
L9	PHY1_RXD[2]	T7	PHY2_RXD[2]
T12	PHY1_RXD[3]	L8	PHY2_RXD[3]
M8	PHY1_TX_CLK	P9	PHY2_TX_CLK
P10	PHY1_TXD[0]	T2	PHY2_TXD[0]
R11	PHY1_TXD[1]	R6	PHY2_TXD[1]
P11	PHY1_TXD[2]	T5	PHY2_TXD[2]
R12	PHY1_TXD[3]	R5	PHY2_TXD[3]
R9	PHY1_TXEN	P5	PHY2_TXEN
P13	PHY1_LINK	T6	PHY2_LINK

Figure 15 : EtherCAT Pin Connection

UART

The OSCAR board has UART connection as show in the Figure 16. There are three plated-through holes (J1) with pitch 2.54 mm that is designed to connect a header connector with pitch 2.54 mm. The OSCAR board also has UART connection to the expansion connector (CN4).

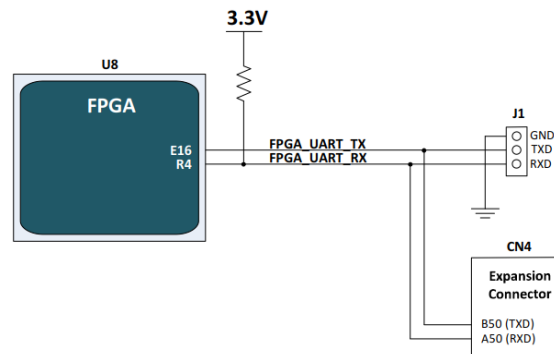


Figure 16 : UART Connection

LED and Switch

The MAX 10 has 1 DIP switch, 1 button switch, 2 rotary switches, and 4 LEDs connection as shown in the Figure 17. The voltage level of all switches and all LEDs is 3.3.V. The DIP switch (SW4) is used to select the configuration image because this MAX 10 has dual configuration image. To manually reset the OSCAR board, press the button switch (SW3) for resetting the system. For the rotary switches (SW1 and SW2), the part number is SD-2110. The MAX will detect real code from the rotary switches to identify the OSCAR board. To detect real code of each rotary switch, it is controlled by output enable of buffer that connected to FPGA IO (x1 for units, x10 for tens). The purpose of LED RUN and ERR is to show the status of EtherCAT. The MAX 10 has to drive high logic to turn on the LEDs, and low logic to turn off the LEDs.

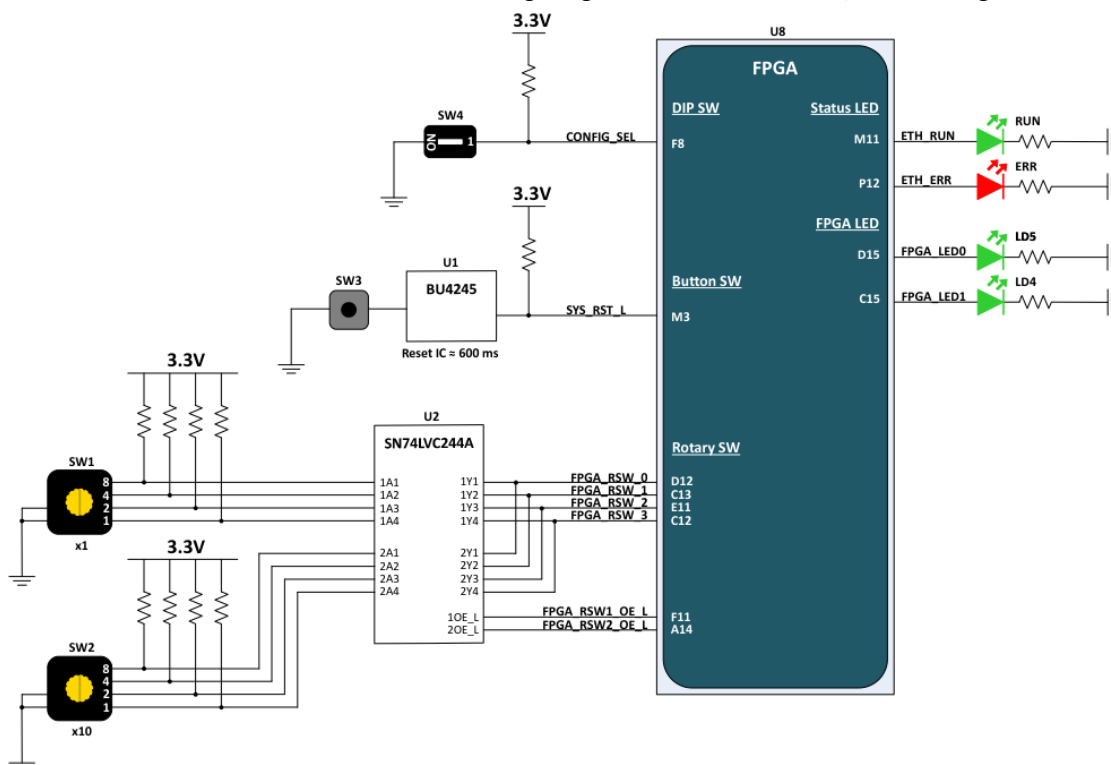


Figure 17 : LED and Switch

The power LED (LD1) indicates the power 5V of the OSCAR board as shown in the Figure 18.

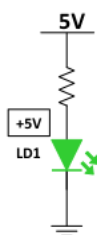


Figure 18 : Power LED

The two LEDs (LD2 and LD3) show the speed of EtherCAT communication as shown in the Figure 19. If LED is ON, the link speed is 100Mbps. If LED is OFF, the speed is 10Mbps.

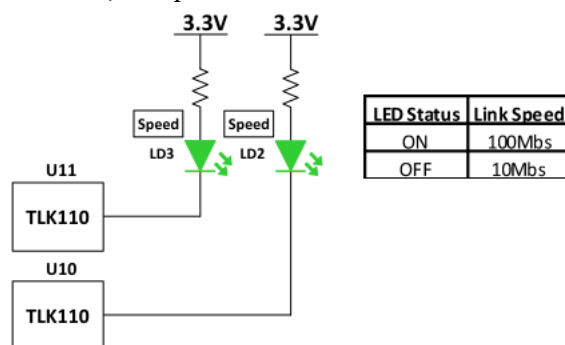


Figure 19 : EtherCAT Speed LED

Expansion IO

The OSCAR board has an expansion connector on the bottom of the board. The IO pins are directly connected to the MAX 10. Voltage level of all IO pins is 3.3V, and IO pins include power, ADDR, DATA, IO, and UART.

Expansion Connection Table

OSCAR CN4					
FPGA Pin	Signal name	CN4		Signal name	FPGA Pin
	5V	A1	B1	5V	
	5V	A2	B2	5V	
	3.3V	A3	B3	3.3V	
	3.3V	A4	B4	3.3V	
F12	FPGA_ADDR2	A5	B5	FPGA_ADDR3	A15
F10	FPGA_ADDR4	A6	B6	FPGA_ADDR5	E10
B13	FPGA_ADDR6	A7	B7	FPGA_ADDR7	A13
D9	FPGA_ADDR8	A8	B8	FPGA_ADDR9	C9
F9	FPGA_ADDR10	A9	B9	FPGA_ADDR11	B12
	GND	A10	B10	GND	
E9	FPGA_ADDR12	A11	B11	FPGA_ADDR13	B11
C10	FPGA_ADDR14	A12	B12	FPGA_ADDR15	A11
B10	FPGA_ADDR16	A13	B13	FPGA_ADDR17	A12
B8	FPGA_ADDR18	A14	B14	FPGA_ADDR19	A10
B7	FPGA_ADDR20	A15	B15	FPGA_ADDR21	A9
B9	FPGA_ADDR22	A16	B16	FPGA_ADDR23	A8
B6	FPGA_ADDR24	A17	B17	FPGA_ADDR25	A7
C6	FPGA_ADDR26	A18	B18	FPGA_ADDR27	A6
B5	FPGA_ADDR28	A19	B19	FPGA_CS_L	N4
	GND	A20	B20	GND	
B4	FPGA_DATA0	A21	B21	FPGA_DATA1	C5
A5	FPGA_DATA2	A22	B22	FPGA_DATA3	A3
A2	FPGA_DATA4	A23	B23	FPGA_DATA5	B3
A4	FPGA_DATA6	A24	B24	FPGA_DATA7	F5
C4	FPGA_DATA8	A25	B25	FPGA_DATA9	F4
C3	FPGA_DATA10	A26	B26	FPGA_DATA11	H5
E3	FPGA_DATA12	A27	B27	FPGA_DATA13	G5
F2	FPGA_DATA14	A28	B28	FPGA_DATA15	G2
C2	FPGA_DATA16	A29	B29	FPGA_DATA17	F1
	GND	A30	B30	GND	
B2	FPGA_DATA18	A31	B31	FPGA_DATA19	E1
B1	FPGA_DATA20	A32	B32	FPGA_DATA21	D1
C1	FPGA_DATA22	A33	B33	FPGA_DATA23	J1
J5	FPGA_DATA24	A34	B34	FPGA_DATA25	H6
J3	FPGA_DATA26	A35	B35	FPGA_DATA27	J2
L1	FPGA_DATA28	A36	B36	FPGA_DATA29	K2
J6	FPGA_DATA30	A37	B37	FPGA_DATA31	M2
L2	FPGA_WE_L0	A38	B38	FPGA_WE_L1	N2
N2	FPGA_WE_L2	A39	B39	FPGA_WE_L3	P1
	GND	A40	B40	GND	
P4	BUF_CTRL1	A41	B41	FPGA_EXT_RST_L	K6
P2	BUF_CTRL2	A42	B42	FPGA_WAIT_L	N1
N5	BUF_CTRL3	A43	B43	FPGA_INT_L	K5
R1	BUF_CTRL4	A44	B44	FPGA_CLK	L6
M6	BUF_CTRL5	A45	B45	FPGA_RD_L	N3
R3	BUF_CTRL6	A46	B46	SYS_RST_L	-
-	-	A47	B47	FPGA_IO0	L7
-	SYS_CLK_25MHz_OUT	A48	B48	FPGA_IO1	R2
-	-	A49	B49	-	-
R4	FPGA_UART_RX	A50	B50	FPGA_UART_TX	T3

Figure 20 : Expansion Connector

FPGA Pin Summary

This is the summary of FPGA pin. For more detail please see on Schematic of OSCAR board.

FPGA Connection Table

Signal name	FPGA Pin	Signal name	FPGA Pin
FPGA_CLK_25MHz	L3	EEPROM	
SYS_RST_L	M3	SCL	D14
JTAGEN	G6	SDA	E16
TCK	H3	Serial NOR Flash	
TDI	G1	SPI_FLASH_DQ0	G12
TDO	H1	SPI_FLASH_DQ1	B16
TMS	H2	SPI_FLASH_DQ2	F14
CONFIG_SEL	F8	SPI_FLASH_DQ3	E15
SDRAM		SPI_FLASH_S_L	E14
SDRAM_ADDR0	P14	EtherCAT	
SDRAM_ADDR1	T14	FPGA_PHY1_2_RESET_L	P6
SDRAM_ADDR2	R14	PHY1_2_MDCLK	R8
SDRAM_ADDR3	T15	PHY1_2_MDIO	T9
SDRAM_ADDR4	L11	PHY1_LINK	P13
SDRAM_ADDR5	L12	PHY1_RX_CLK	M9
SDRAM_ADDR6	N14	PHY1_RX_DV	T11
SDRAM_ADDR7	M15	PHY1_RX_ER	R10
SDRAM_ADDR8	P15	PHY1_RXD[0]	M10
SDRAM_ADDR9	M14	PHY1_RXD[1]	T13
SDRAM_ADDR10	N16	PHY1_RXD[2]	L9
SDRAM_ADDR11	R15	PHY1_RXD[3]	T12
SDRAM_ADDR12	P16	PHY1_TX_CLK	M8
SDRAM_BA0	R16	PHY1_TXD[0]	P10
SDRAM_BA1	K11	PHY1_TXD[1]	R11
SDRAM_CAS_L	K12	PHY1_TXD[2]	P11
SDRAM_CKE	L16	PHY1_TXD[3]	R12
SDRAM_CS_L	L15	PHY1_TXEN	R9
SDRAM_DQ0	J12	PHY2_LINK	T6
SDRAM_DQ1	K15	PHY2_RX_CLK	P8
SDRAM_DQ2	J15	PHY2_RX_DV	R7
SDRAM_DQ3	H15	PHY2_RX_ER	T8
SDRAM_DQ4	J16	PHY2_RXD[0]	T4
SDRAM_DQ5	H16	PHY2_RXD[1]	M7
SDRAM_DQ6	D16	PHY2_RXD[2]	T7
SDRAM_DQ7	C16	PHY2_RXD[3]	L8
SDRAM_DQ8	H11	PHY2_TX_CLK	P9
SDRAM_DQ9	H12	PHY2_TXD[0]	T2
SDRAM_DQ10	G14	PHY2_TXD[1]	R6
SDRAM_DQ11	G16	PHY2_TXD[2]	T5
SDRAM_DQ12	G15	PHY2_TXD[3]	R5
SDRAM_DQ13	F16	PHY2_TXEN	P5
SDRAM_DQ14	G11	LED	
SDRAM_DQ15	B15	ETH_ERR	P12
SDRAM_DQMH	J14	ETH_RUN	M11
SDRAM_DQML	J11	FPGA_LED0	D15
SDRAM_RAS_L	K14	FPGA_LED1	C15
SDRAM_WE_L	M16		

Signal name	FPGA Pin	Signal name	FPGA Pin
Rotary Switch		GPIO	
FPGA_RSW1_OE_L	F11	FPGA_DATA4	A2
FPGA_RSW2_OE_L	A14	FPGA_DATA5	B3
FPGA_RSW_0	D12	FPGA_DATA6	A4
FPGA_RSW_1	C13	FPGA_DATA7	F5
FPGA_RSW_2	E11	FPGA_DATA8	C4
FPGA_RSW_3	C12	FPGA_DATA9	F4
GPIO		FPGA_DATA10	C3
BUF_CTRL1	P4	FPGA_DATA11	H5
BUF_CTRL2	P2	FPGA_DATA12	E3
BUF_CTRL3	N5	FPGA_DATA13	G5
BUF_CTRL4	R1	FPGA_DATA14	F2
BUF_CTRL5	M6	FPGA_DATA15	G2
BUF_CTRL6	R3	FPGA_DATA16	C2
FPGA_ADDR2	F12	FPGA_DATA17	F1
FPGA_ADDR3	A15	FPGA_DATA18	B2
FPGA_ADDR4	F10	FPGA_DATA19	E1
FPGA_ADDR5	E10	FPGA_DATA20	B1
FPGA_ADDR6	B13	FPGA_DATA21	D1
FPGA_ADDR7	A13	FPGA_DATA22	C1
FPGA_ADDR8	D9	FPGA_DATA23	J1
FPGA_ADDR9	C9	FPGA_DATA24	J5
FPGA_ADDR10	F9	FPGA_DATA25	H6
FPGA_ADDR11	B12	FPGA_DATA26	J3
FPGA_ADDR12	E9	FPGA_DATA27	J2
FPGA_ADDR13	B11	FPGA_DATA28	L1
FPGA_ADDR14	C10	FPGA_DATA29	K2
FPGA_ADDR15	A11	FPGA_DATA30	J6
FPGA_ADDR16	B10	FPGA_DATA31	M2
FPGA_ADDR17	A12	FPGA_CLK	L6
FPGA_ADDR18	B8	FPGA_CS_L	N4
FPGA_ADDR19	A10	FPGA_EXT_RST_L	K6
FPGA_ADDR20	B7	FPGA_INT_L	K5
FPGA_ADDR21	A9	FPGA_IO0	L7
FPGA_ADDR22	B9	FPGA_IO1	R2
FPGA_ADDR23	A8	FPGA_RD_L	N3
FPGA_ADDR24	B6	FPGA_WAIT_L	N1
FPGA_ADDR25	A7	FPGA_WE_L0	L2
FPGA_ADDR26	C6	FPGA_WE_L1	N2
FPGA_ADDR27	A6	FPGA_WE_L2	M1
FPGA_ADDR28	B5	FPGA_WE_L3	P1
FPGA_DATA0	B4	UART	
FPGA_DATA1	C5	FPGA_UART_RX	R4
FPGA_DATA2	A5	FPGA_UART_TX	T3
FPGA_DATA3	A3		

Figure 21 : FPGA Connection Summary

Start Using OSCAR

Power Up the OSCAR Board

Firstly, plug the power supply in to CN1, and see the LED beside the connector. LD1 should be bright. The Figure 22 shows the location of power connector, power on LED, and power test points.

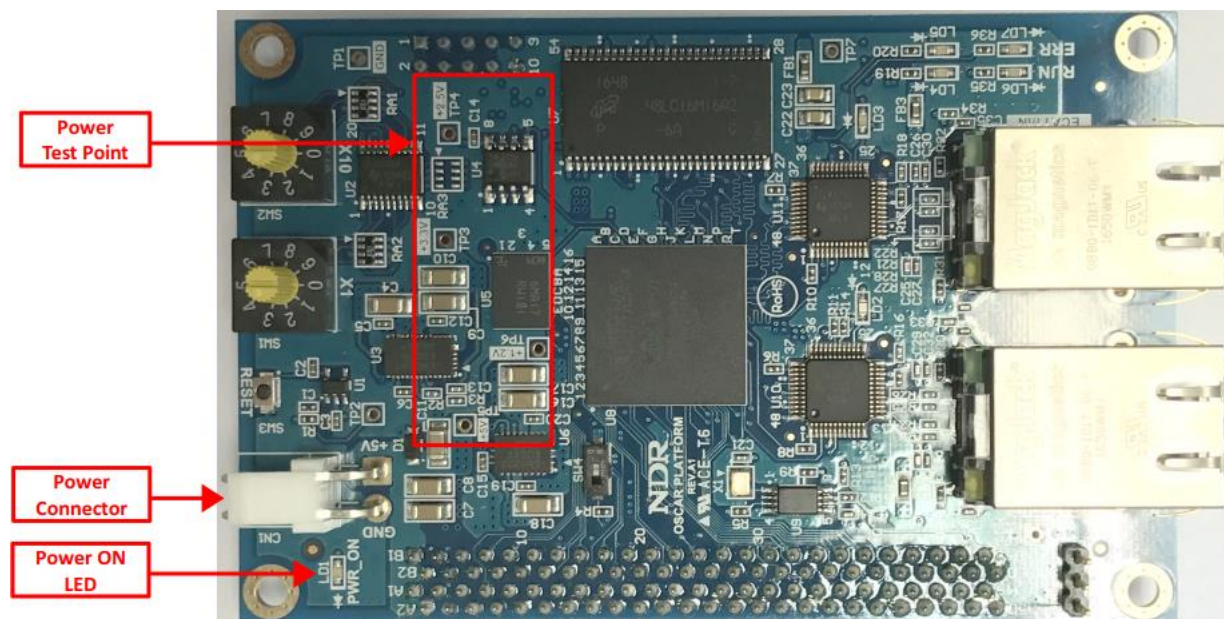


Figure 22 : Location of OSCAR Power

Design and Program

Platform that may include NIOS core can be created from QSYS tool. and adds the platform to the MAX 10. The programmer of Quartus Prime is used to program MAX 10 via JTAG connector.

Associated Product

ZEKE Board

ZEKE board is an evaluation board which contains Cyclone V System-on-Chip (SoC), DDR3 memory, two of 10/100/1000 Ethernet (PHY), two of 10/100 Ethernet (PHY), MicroSD Card connector, NOR flash memory along with user IO such as DIP switch, LED, and expansion connector. For more information please see on ZEKE Board User Manual. The look of the ZEKE board is shown in the Figure 23.



Figure 23 : ZEKE Board

Additional Information

Getting Help

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Web: <http://ndr.co.jp/en/>

Revision History

Date	Revision	Changes list
2017-10-05	0.1	First draft